SHARP

SERVICE MANUAL

SE00LC32GD900
Issued: 20th June 2006

LCD COLOUR TELEVISION

PAL B/G, I / SECAM B/G, D/K, L/L' SYSTEM COLOUR TELEVISION

MODELS

LC-32GD9EE/F/I/K/RU
LC-37GD9EE/F/I/K/RU

In the interests of user safety (required by safety regulations in some countries) the set should be restored to its original condition and only parts identical to those specified should be used.

CONTENTS

SHARP CORPORATION

MAJOR ICs INFORMATION

1. General ICs Information

XD890WJ (MAIN UNIT):

· **IC1905** : HDMI RECEIVER
Part number: Sii9021
Sharp code: VHISII9021+-1Q
The Sii9021 is a second generation panel link cinema receiver that is compatible with the HDMI 1.1 (High Definition Multimedia Interface) specification. The Sii9021 is capable of receiving and outputting two channel digital audio signals at up to 192 kHz— an excellent solution for digital TVs.
This IC features the following.
1) Digital video interface supports video processors.
2) Analog RGB and YPbPr output: 10-bit DAC.
3) Digital audio interface supports high-end audio systems.

· **IC1901 & IC1902**: NVM OF HDMI (E-EDID)
Part number: 24LC2BIN
Sharp code: VHI24LC2BIN-1Y
This IC is a 2-wire (I2C bus type) serial EEPROM this is electrically programmable. This EEPROM chip stores the data structure used to carry configuration information for optimal use of a display (EDID data).

· **IC2701** : SYNC SELECT
Part number: TVHC153T
Sharp code: VHITVHC153T-1Y
This VHC153 is a high-speed Dual 4-input multiplexer with common select inputs and individual enable inputs for each section.

· **IC2704** : HDMI & RGB SOUND MULTIPLEXER
Part number: CD4052BP
Sharp code: VHICD4052BP-1Y
The TC74HC4052A is a high-speed CMOS analog multiplexer/demultiplexer backed by silicon gate CMOS technology. The multiplexer function includes the selection and mixing of analog and digital signals. The chip consists of 4 channels (x 2). A digital signal through the control terminal turns on the switch of a corresponding channel.

· **IC3002 :** VIDEO PROCESSOR
Part number: VCTP
Sharp code: RH-IXB698WJZZQ
The VCT 6wxyP family is dedicated to high-quality FPD and double-scan TV sets. The memory and program ROM are integrated in the IC. Modular design and deep submicron technology allow the integration of audio, video, teletext, OSD, and controller-related functionalities. They cover the whole range of flat-panel display TVs. The IC is based on proven functional blocks of existing products like VCT 49xxI, VSP 94x5B, and DPS 94xxB.
Each member of the IC family contains the entire audio, video, upconversion processing for 4:3 and 16:9 50/60 Hz progressive or 100/120 Hz interlaced stereo TV sets plus the control/data interface for flat-panel displays. The integrated microcontroller is supported by a powerful OSD and graphics generator with integrated teletext acquisition.
The VCT 6wxyP family provides a front-end video processing unit with 4 CVBS-Y/C or component inputs for HDTV, EDTV, and SDTV. A VBI slicer, support of 1000 pages of teletext, and a 3-D comb filter for PAL and NTSC (in certain versions) are also available. The front-end unit further allows to process an SD and an HD source in parallel, thus enabling PiP and PaP functionality. Motion-adaptive de-interlacing, temporal noise reduction, and film mode detection are based on a unified memory technology.
Post-scaling in the display processing block ensures the desired output format. Display processing is supported by an 8-bit 8051-compatible controller. By means of powerful alpha-blending, the graphics mixer composes the output image from following image layers: the video layer, the OSD layer and the pixel graphics layer.
The audio part consists of a multistandard sound IF demodulator and a baseband processor supporting all desired sound features in this range.
A connection for additional features, such as advanced motion compensation via -Micronas' FRC 94xyA, is also provided.

· **IC2702 & IC2705:** VIDEO INPUT SELECTOR.
Part number: MM1507XN
Sharp code: VHIMM1507XN-1Y
This IC extends the series of ICs for video/audio signal switching, with a 2-input 1-output single video switch with 75Ω driver and input clamp.

· **IC3001 :** NVM 64Kb-E2PROM
Part number: BR24L64F
Sharp code: VHIBR24L64F-1Y
The BR24L64F is a 2-wire (I2C bus type) serial EEPROM that is electrically programmable. This IC stores the control data of system contents (last memory, for example) for the main microprocessor's AV PWB and main PWB. The data is given out by commands from the main microprocessor.

· **IC3003 :** PIC MICROCONTROLLER
Part number: PIC16F913
Sharp code: RH-IXB664WJZZY
28 Pin Flash-Based, 8 bit CMOS Microcontrollers with LCD Driver and nanoWatt Technology.
This IC is controlled via I2C and works how expander of ports. This IC has led control and include A/D converter.

· **IC3005**: RESET IC FOR VCTP (IC3002)
Part number: BU4215G
Sharp code: VHIBU4215G+-1Y
Low voltage detector IC with adjustable output delay. Standard detection voltage = 1.5V

· **IC3301:** HIGH-END FRAME-RATE CONVERTER
Part number: FRC 942xA
Sharp code: RH-IXB064WJN1Q
The FRC 942xA is a single-chip frame rate converter with vector-based motion compensation, video scaling, and high-performance picture improvement features. It integrates all functions – including all video frame buffers – in one monolithic IC.

· **IC3302**: RESET IC FOR FRC (IC3301).
Part number: BU4215G
Sharp code: VHIBU4215G+-1Y
Low voltage detector IC with adjustable output delay. Standard detection voltage = 1.5V

· **IC2301 :** RS-232 TRANSMITTERS/RECEIVERS
Part number: ISL83220
Sharp code: VHIISL83220-1Y
The ISL83220E is a 3.0V to 5.5V powered RS-232 transmitter/receiver,+/-15kV ESD protected, minimum data rate 250 kpbs.

· **IC2303 :** NVM OF PC MODE (EDID)
Part number: BR24C21F
Sharp code: VHIBR24C21F-1Y
This IC is a 2-wire (I2C bus type) serial EEPROM this is electrically programmable. This EEPROM chip stores the data structure used to carry configuration information for optimal use of a display (EDID data).

· **IC1701:** POWER RESET OF +BU1.8V
Part number: BU4239G
Sharp code: VHIBU4239G+-1Y
Low voltage detector IC with adjustable output delay. Standard Detection Voltage = 3.9V

· **IC1702:** BU+3.3V (VOLTAGE INPUT: BU+5V)
Part number: PQ20WZ11
Sharp code: VHIPQ20WZ11-1Y
Low power-loss voltage regulators. Variable Output. Output current 1A. Built-in overcurrent, overheat protection functions, ASO protection circuit.

· **IC1703:** S+8V (VOLTAGE INPUT: POW+12V)
Part number: PQ20WZ11
Sharp code: VHIPQ20WZ11-1Y
Low power-loss voltage regulators. Variable Output. Output current 1A. Built-in overcurrent, overheat protection functions, ASO protection circuit.

· **IC1707:** +3.3V (VOLTAGE INPUT: POW+5V)
Part number: PQ20WZ11
Sharp code: VHIPQ20WZ11-1Y
Low power-loss voltage regulators. Variable Output. Output current 1A. Built-in overcurrent, overheat protection functions, ASO protection circuit.

· **IC1708:** +1.8V (VOLTAGE INPUT: POW+5V)
Part number: MP1410
Sharp code: VHIMP1410ES-1Y
DC to DC Converter. 2A Step down switch mode regulator with a built in internal Power Mosfet. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

· **IC1706:** BU+1.8V (VOLTAGE INPUT: BU+5V)
Part number: MP1410
Sharp code: VHIMP1410ES-1Y
DC to DC Converter. 2A Step down switch mode regulator with a built in internal Power Mosfet. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

· **IC1710:** CPLD
Part number: EPM240T
Sharp code: RH-IXB823WJZZQ
This IC is a CPLD of Altera MAXII family and use 240 logic elements (LEs) (192 equivalent macrocells)
MAX II devices offer high I/O counts, fast performance. MAX II devices are designed to reduce cost and power while providing programmable solutions for applications such as bus bridging, I/O expansion, power-on reset (POR) and sequencing control, and device configuration control.
This device controls ON/OFF power supply, signals for inverter unit and etc.

FD604WJ (AV UNIT):

· **IC301 & IC302** : AUDIO AMPLIFIER
Part number: TDA8931T
Sharp code: VHITDA893T-1Y
The TDA8931 is a switching power stage for high efficiency class-D audio power amplifier systems. The IC has a high efficiency so that a heat sink is not required up to 20W (RMS).

· **IC303** : HEADPHONE AMPLIFIER
Part number: NJM4558M
Sharp code: VHINJM4558M-1Y
The NJM4558 is a dual high-gain operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

IC1101 & IC1102: SCART VIDEO OUTPUT DRIVER.
Part number: MM1506XN
Sharp code: VHIMM1506XN-1Y
This IC extends the series of ICs for video/audio signal switching, with a 2-input 1-output single video switch with 75Ω driver and input bias (6dB gain).

IC1201: VIDEO INPUT SELECTOR.
Part number: MM1507XN
Sharp code: VHIMM1507XN-1Y
This IC extends the series of ICs for video/audio signal switching, with a 2-input 1-output single video switch with 75Ω driver and input clamp.

FD605WJ (POWER SUPPLY UNIT):

· **IC704:** POWER SUPPLY CONTROLLER FOR SIGNAL BOARD
Part number: MR4030
Sharp code: VHIMR4030++-1
A high speed 900V IGBT makes ideal partial resonance operation which ensures high efficiency and low noise.
Very low power consumption at micro-loads (burst mode).
Start-up circuit eliminates the need for start-up resistor.
Excess current protection (ON period limitation, primary current limitation), excess voltage protection, and thermal shut-down function are incorporated.

· **IC705:** POWER SUPPLY CONTROLLER FOR INVERTER
Part number: MR4020
Sharp code: VHIMR4020++-1
A high speed 900V IGBT makes ideal partial resonance operation which ensures high efficiency and low noise.
Very low power consumption at micro-loads (burst mode).
Start-up circuit eliminates the need for start-up resistor.
Excess current protection (ON period limitation, primary current limitation), excess voltage protection, and thermal shut-down function are incorporated.

· **IC706 & IC707:** FEEDBACK CONTROL
Part number: TA76431R
Sharp code: VHITA76431R-1Y
Adjustable precision shunt regulator for feedback control for driving an optocoupler in power supplies

IC708: LOW AC MAINS VOLTAGE DETECTOR.
Part number: NJM2904M
Sharp code: VHINJM2904M-1Y
The IC consists of two independent, high gain internally frequency compensated operation amplifiers which were designed specifically to operate from single power supply.

IC709: +24V/+5V VOLTAGE SUPERVISOR.
Part number: NJM2903M
Sharp code: VHINJM2903M-1Y
The IC consist of two independent precision voltage comparator, high gain internally frequency compensated operation amplifiers which were designed specifically to operate from single power supply.

FD607WJ (RC/LED UNIT):

· **IC101 :** OPC
Part number: TPS850
Sharp code: VHITPS850++-1Y
The TPS850 is a linear-output photo-IC which incorporates a photodiode and current amp circuit in a single chip. This photo-IC is current output type, so can set up output voltage freely by arbitrary load resistance.

FD609WJ (TUNER UNIT):

· **IC201 :** IF-Demodulator/PLL
Part number: TDA9886
Sharp code: VHITDA9886+-1Y
The TDA9886 is an alignment-free multi-standard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation including sound AM and FM processing.
This IC features are the following.
* Gain controlled wide-band vision intermediate frequency (VIF) amplifier (AC-coupled).
* Multi-standard true synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures reduced harmonics, excellent pulse response).
* Gate phase detector for L/L accent standard.
* Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free; frequencies switchable for all negative modulated standards via I2C bus.

* 4MHz reference frequency input [signal from phase-locked loop (PLL) tuning system] or operating as crystal oscillator.
* VIF Automatic Gain Control (AGC) detector for gain control operating as a peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals.

IC 202: COFDM DECODER.
Part number: STV0360C
Sharp code: RH-IXB682WJZZQ
The STV0360C is a COFDM (codec orthogonal frequency division multiplex) demodulator that performs IF to MPEG-2 block processing of OFDM carriers. It is intended for digital terrestrial receivers for compressed video, sound and data services. It implements all the functions from the tuner IF output to the MPEG-2 transport stream input. The STV0360C integrates an A/D converter that delivers the required performance to handle up to 64 QAM carriers in a direct IF sampling architecture.

IC204: I2C BUS SELECTOR (TUNER CONTROLLED FROM VCTP OR COFDM DECODER).
Part number: SN74LV4053APWR
Sharp code: VHILV4053AT-1Y
The SN74LV4053APWR is a high-speed CMOS analog multiplexer/demultiplexer backed by silicon gate CMOS technology. The multiplexer function includes the selection and mixing of analog and digital signals. The chip include two independent 3 channels selectors. A digital signal through the control terminal turns on the switch of a corresponding channel.

KD628WJ (DIGITAL UNIT):

IC4001: DIGITAL PROCESSOR MPEG 1/2 DECODER (Audio/Video).
Part number: STI5516AUCL
Sharp code: RH-IXB680WJZZQ
The STi5516 is a device that integrates all of the back-end functions required for mainstream set-top boxes . These include:
*An enhanced ST20 32-bit RISC CPU with a 166MHz clock, 8Kbytes of instruction cache, 8Kbytes of data cache and 8Kbytes of embedded SRAM.
*A 16-bit, 133MHz Shared Memory Interface, with support for 64- and 128-bit configurations.
*A programmable External Memory Interface supporting six separately configurable banks of SRAM, Flash and DRAM.
*An MPEG-2 (MP@ML) decoder, including trick modes such as smooth fast-forward and rewind.
*A Graphics/Display unit with five display panes, alpha blending, antialiasing and antiflutter filters, subpicture decoder, and display compositor with separate OSD (On-Screen Display) controls for TV and VCR outputs.
PAL/NTSC/SECAM encoder.
*Audio subsystem with embedded DSP for all popular audio formats.
*A full range of on-chip peripherals, including five UARTs, six parallel I/O banks, two smart card interfaces, four PWM channels, teletext serializer, multi-channel IR transmitter/receiver, and a modem analog front-end interface.

IC 4203: 16 Mbit Flash Memory (Program Memory).
Part number: MBM29LV160BE70TN
Sharp code: RH-IXA964WJN1

IC 4201 & IC 4202: 64Mbit SDRAM (Temporary Data).
Part number: KAS641632H-UC75
Sharp code: RH-IXB076WJZZQ

IC4204: NVM 64Kb-E2PROM FOR DIGITAL PROCESSOR (IC4001).
Part number: BR24L64F
Sharp code: VHIBR24L64F-1Y
The BR24L64F is a 2-wire (I2C bus type) serial EEPROM that is electrically programmable. This IC stores all data related to the Digital Module (Channels, User settings, etc.).

IC4003: RESET ICs FOR DIGITAL PROCESSOR (IC4001).
Part number: BU4228G
Sharp code: VHIBU4228G+-1Y
Low voltage detector IC with adjustable output delay. Standard detection voltage = 2.8V.

IC4402 & IC4405: OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS.
Part number: SN74LVC573APWR
Sharp code: VHILVC573AP-1Y
These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers. In this design additionally are isolating digital processor (IC4001) from PCMCIA connector.

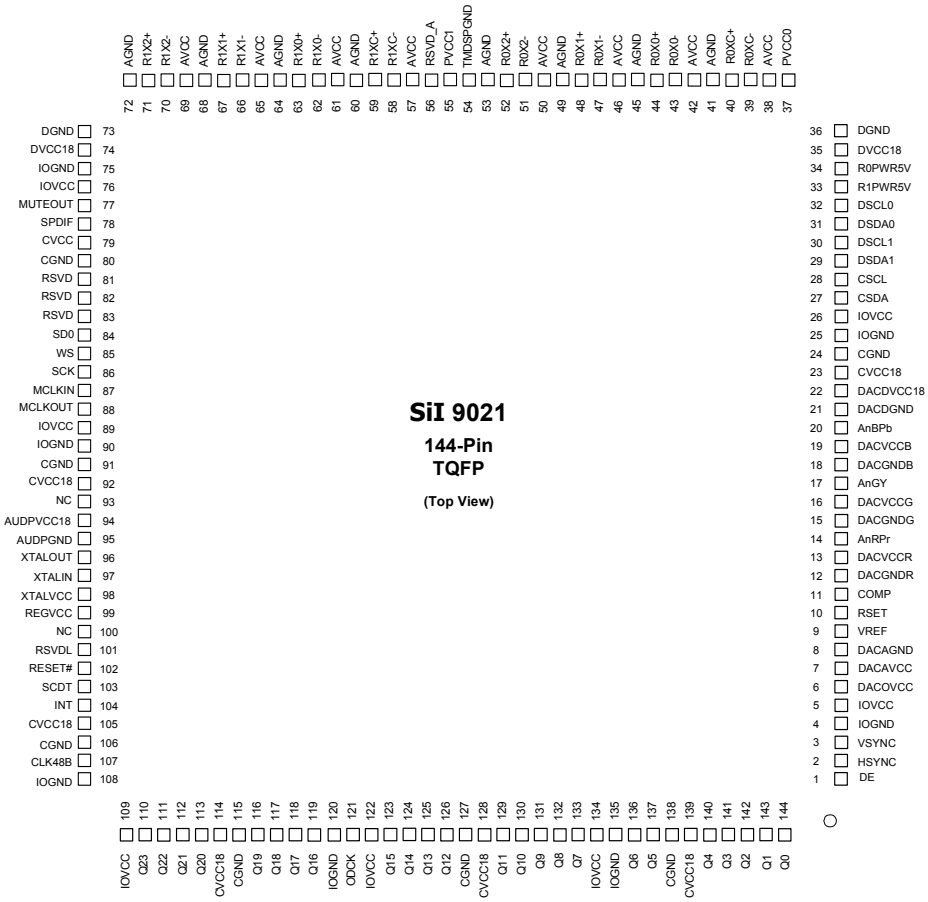
IC4401: LOW VOLTAGE OCTAL BUS TRANSCEIVER WITH 5V TOLERANT INPUTS AND OUTPUTS.
Part number: TC74LCX245FS
Sharp code: VHICLCX245-2Y
The device is designed for working in 3.3V systems but could be used to interface to 5V supply environment for both inputs and outputs. The direction of the data transmission is controlled by the level of the DIR input. The OE input could be used to isolate the device of the busses (PCMCIA and Digital Processor).

IC4404: LOW VOLTAGE BUFFER / LINE DRIVER WITH 5V TOLERANT INPUTS AND OUTPUTS.
Part number: 74LCX244AE
Sharp code: VHILCX244MT-1Y
The LCX244 contains eight non-inverting buffers with 3-STATE outputs. The device may be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver. The LCX244 is designed for low voltage (2.5V or 3.3V) VCC applications with capability of interfacing to a 5V signal environment.

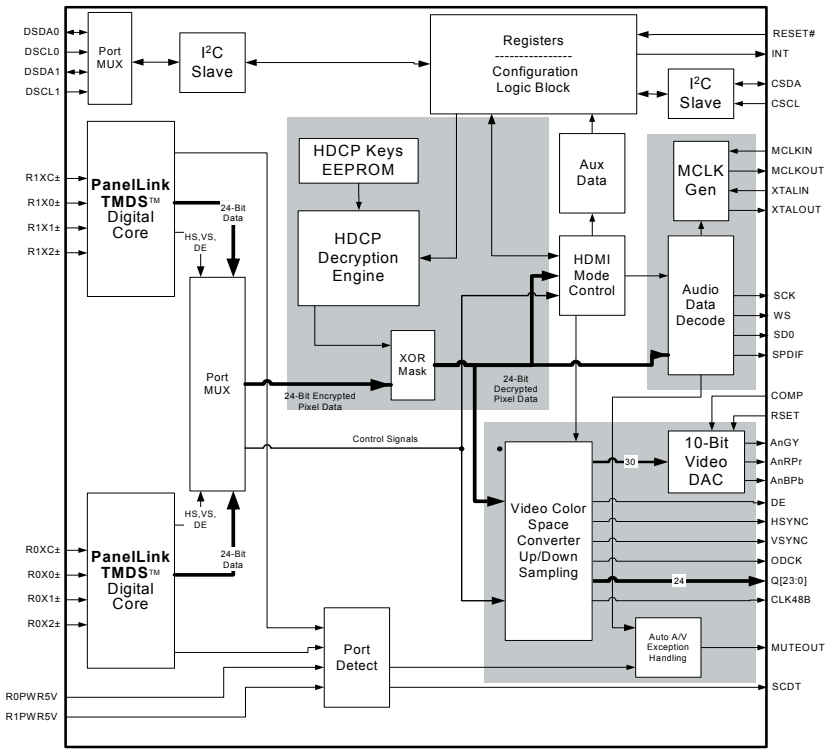
2. Detailed ICs Information

2.1. IC1905 (VHISII9021+-1Q)

2.1.1. Pinning



2.1.2. Block Diagram



The SiI 9021 supports two HDMI input ports. Only one port may be active at any time.

2.2. IC3002 (RH-IXB698WJZZQ)

2.2.1. Pin Connections and Short Description

IN = Input Pin
ANA = Analog Pin
OUT = Output Pin
SUPPLY = Supply Pin

NC = not connected
LV = if not used, leave vacant
OBL = obligatory; connect as described in circuit diagram

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
1		656O6 P4_6 TDOFW	IN/OUT	LV	Digital 656 Bit 6 Output Port 4, Bit 6 Input/Output JTAG Interface Data Output (firmw. Controler)
2		656O5 P4_5 TDIFW	IN/OUT	LV	Digital 656 Bit 5 Output Port 4, Bit 5 Input/Output JTAG Interface Data Input (firmw. Controler)
3		656O4 P4_4 TMSFW	IN/OUT	LV	Digital 656 Bit 4 Output Port 4, Bit 4 Input/Output JTAG Interface Mode Select Input (fw. Contr.)
4		656O3 P4_3 TCLK	IN/OUT	LV	Digital 656 Bit 3 Output Port 4, Bit 3 Input/Output JTAG Interface Clock Input (TV Controler)
5		656O2 P4_2 TDO	IN/OUT	LV	Digital 656 Bit 2 Output Port 4, Bit 2 Input/Output JTAG Interface Data Output (TV Controler)
6		656O1 P4_1 TDI	IN/OUT	LV	Digital 656 Bit 1 Output Port 4, Bit 1 Input/Output JTAG Interface Data Input (TV Controler)
7		656O0 P4_0 TMS	IN/OUT	LV	Digital 656 Bit 0 Output (LSB) Port 4, Bit 0 Input/Output JTAG Interface Mode Select Input (TV Contr.)
8		RESETQ	IN/OUT	OBL	$\overline{\text{Reset}}$ Input/Output
9		AIN1R	IN	GND	Analog Audio 1 Input, Right
10		AIN1L	IN	GND	Analog Audio 1 Input, Left
11		AIN2R	IN	GND	Analog Audio 2 Input, Right
12		AIN2L	IN	GND	Analog Audio 2 Input, Left
13		AIN3R	IN	GND	Analog Audio 3 Input, Right
14		AIN3L	IN	GND	Analog Audio 3 Input, Left
15		AIN4R	IN	GND	Analog Audio 4 Input, Right
16		AIN4L	IN	GND	Analog Audio 4 Input, Left
17		VREFAU	ANA	OBL	Reference Voltage, Audio
18		VSUP8.0AU	SUPPLY	OBL	Supply Voltage Analog Audio, 8.0 V
19		GNDA	SUPPLY	OBL	Ground Analog Audio, Platform Ground
20		SGND	ANA	OBL	Analog Signal GND

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
21		AOUT2R AIN5R	IN/OUT	LV	Analog Audio 2 Output, Right Analog Audio 5 Input, Right
22		AOUT2L AIN5L	IN/OUT	LV	Analog Audio 2 Output, Left Analog Audio 5 Input, Left
23		AOUT1R	OUT	LV	Analog Audio 1 Output, Right
24		AOUT1L	OUT	LV	Analog Audio 1 Output, Left
25		HEADPHONER	OUT	LV	Analog Headphone Output, Right
26		HEADPHONEL	OUT	LV	Analog Headphone Output, Left
27		SPEAKERR	OUT	LV	Analog Loudspeaker Output, Right
28		SPEAKERL	OUT	LV	Analog Loudspeaker Output, Left
29		SUBWOOFER TEST	IN/OUT	LV	Analog SUBWOOFER Output Test Input
30		VREFSIF	ANA	OBL	Reference Voltage, Audio SIF
31		SIFIN+	IN	$VREF_{IF}$	Differential IF Input
32		SIFIN-	IN	$VREF_{IF}$	Differential IF Input
33		VSUP5.0SIF	SUPPLY	OBL	Supply Voltage Analog SIF, 5.0 V
34		GNDA	SUPPLY	OBL	Ground Analog SIF, Platform Ground
35		GND3.3DIG	SUPPLY	OBL	Ground Digital Audio Core
36		VSUP3.3DIG	SUPPLY	OBL	Supply Voltage Digital Audio Core, 3.3 V
37		SPDIF_OUT	OUT	LV	SPDIF Output
38		I2S_DA_IN	IN	LV	Audio Bus Data Input
39		I2S_CL	IN	LV	Audio Bus Clock Input
40		I2S_WS	IN	LV	Audio Bus Word Strobe Input
41		I2S_DEL_OUT	OUT	LV	Audio Delay Line Bus Data Output
42		I2S_DEL_IN	IN	LV	Audio Delay Line Bus Data Input
43		I2S_DEL_CL	OUT	LV	Audio Delay Line Bus Clock Output
44		I2S_DEL_WS	OUT	LV	Audio Delay Line Bus Word Strobe Output
45		VSUP3.3RAM	SUPPLY	OBL	Supply Voltage Ram, 3.3 V
46		GND3.3RAM	SUPPLY	OBL	Ground Ram
47		DVS	IN	LV	Digital or Analog Video VSYNC HD Input
48		DEN	IN	LV	Digital Video Enable Input
49		DCLK	IN	LV	Digital Video Clock Input
50		DRI7	IN	LV	Digital Video Red 7 Input

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
51		DRI6	IN	LV	Digital Video Red 6 Input
52		DRI5	IN	LV	Digital Video Red 5 Input
53		DRI4	IN	LV	Digital Video Red 4 Input
54		DRI3	IN	LV	Digital Video Red 3 Input
55		DRI2	IN	LV	Digital Video Red 2 Input
56		DRI1	IN	LV	Digital Video Red 1 Input
57		DRI0	IN	LV	Digital Video Red 0 Input (LSB)
58		DGI7	IN	LV	Digital Video Green 7 Input
59		DGI6	IN	LV	Digital Video Green 6 Input
60		DGI5	IN	LV	Digital Video Green 5 Input
61		DGI4	IN	LV	Digital Video Green 4 Input
62		DGI3	IN	LV	Digital Video Green 3 Input
63		DGI2	IN	LV	Digital Video Green 2 Input
64		DGI1	IN	LV	Digital Video Green 1 Input
65		DGI0	IN	LV	Digital Video Green 0 Input (LSB)
66		DBI7	IN	LV	Digital Video Blue 7 Input
67		DBI6	IN	LV	Digital Video Blue 6 Input
68		DBI5	IN	LV	Digital Video Blue 5 Input
69		DBI4	IN	LV	Digital Video Blue 4 Input
70		DBI3	IN	LV	Digital Video Blue 3 Input
71		DBI2	IN	LV	Digital Video Blue 2 Input
72		DBI1	IN	LV	Digital Video Blue 1 Input
73		DBI0	IN	LV	Digital Video Blue 0 Input (LSB)
74		GND3.3DRI	SUPPLY	OBL	Ground Digital Ram Interface
75		VSUP3.3DRI	SUPPLY	OBL	Supply Voltage Digital Ram Interface, 3.3 V
76		GND3.3COM	SUPPLY	OBL	Ground Common
77		VSUP3.3COM	SUPPLY	OBL	Supply Voltage Common, 3.3V
78		XTALIN	IN	OBL	Analog Crystal Input
79		XTALOUT	OUT	OBL	Analog Crystal Output
80		CLKOUT	OUT	LV	Digital 20MHz Clock Output
81		VSO	OUT	LV	Vertical Sync Output, Frontend

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
82		HSO	OUT	LV	Horizontal Sync Output, Frontend
83		SCL	IN/OUT	OBL	I^2C Bus Clock Input/Output
84		SDA	IN/OUT	OBL	I^2C Bus Data Input/Output
85		GND3.3FL	SUPPLY	OBL	Ground Flash
86		VSUP3.3FL	SUPPLY	OBL	Supply Voltage Flash, 3.3 V
87		P2_0	IN/OUT	LV	Port 2, Bit 0 Input/Output
88		P2_1	IN/OUT	LV	Port 2, Bit 1 Input/Output
89		P2_2	IN/OUT	LV	Port 2, Bit 2 Input/Output
90		P2_3	IN/OUT	LV	Port 2, Bit 3 Input/Output
91		P2_4 TDI	IN/OUT	LV	Port 2, Bit 4 Input/Output JTAG Interface Data Input
92		P2_5 TMS	IN/OUT	LV	Port 2, Bit 5 Input/Output JTAG Interface Mode Select Input
93		OSDV DBO2_0	IN/OUT	LV	Graphic Vertical Sync Input/Output Channel 2 Digital 0 Blue Output (LSB)
94		OSDH DBO2_1	IN/OUT	LV	Graphic Horizontal Sync Input/Output Channel 2 Digital 1 Blue Output
95		GND3.3IO1	SUPPLY	OBL	Ground Digital Input/Output Port 1
96		VSUP3.3IO1	SUPPLY	OBL	Supply Voltage Input/Output Port 1, 3.3 V
97		OSDCLK DBO2_2	IN/OUT	LV	Graphic Clock Input/Output Channel 2 Digital 2 Blue Output
98		OSDFSW DBO2_3	IN/OUT	LV	Graphic Fast Switch Input/Output Channel 2 Digital 3 Blue Output
99		OSDHCS1 P3_7 DBO2_4	IN/OUT	LV	Graphic Half Contrast 1 Input/Output Port 3, Bit 7 Input/Output Channel 2 Digital 4 Blue Output
100		OSDHCS0 P3_6 DBO2_5	IN/OUT	LV	Graphic Half Contrast 0 Input/Output (LSB) Port 3, Bit 6 Input/Output Channel 2 Digital 5 Blue Output
101		OSDB3 P3_5 DBO2_6	IN/OUT	LV	Graphic Blue 3 Input/Output (MSB) Port 3, Bit 5 Input/Output Channel 2 Digital 6 Blue Output
102		OSDB2 P3_4 DBO2_7	IN/OUT	LV	Graphic Blue 2 Input/Output Port 3, Bit 4 Input/Output Channel 2 Digital 7 Blue Output (MSB)
103		OSDB1 DGO2_0	IN/OUT	LV	Graphic Blue 1 Input/Output Channel 2 Digital 0 Green Output (LSB)
104		OSDB0 DGO2_1	IN/OUT	LV	Graphic Blue 0 Input/Output Channel 2 Digital 1 Green Output

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
105		OSDG3 P3_3 DGO2_2	IN/OUT	LV	Graphic Green 3 Input/Output (MSB) Port 3, Bit 3 Input/Output Channel 2 Digital 2 Green Output
106		OSDG2 P3_2 DGO2_3	IN/OUT	LV	Graphic Green 2 Input/Output Port 3, Bit 2 Input/Output Channel 2 Digital 3 Green Output
107		OSDG1 DGO2_4	IN/OUT	LV	Graphic Green 1 Input/Output Channel 2 Digital 4 Green Output
108		OSDG0 DGO2_5	IN/OUT	LV	Graphic Green 0 Input/Output Channel 2 Digital 5 Green Output
109		OSDR3 P3_1 DGO2_6	IN/OUT	LV	Graphic Red 3 Input/Output (MSB) Port 3, Bit 1 Input/Output Channel 2 Digital 6 Green Output
110		OSDR2 P3_0 DGO2_7	IN/OUT	LV	Graphic Red 2 Input/Output Port 3, Bit 0 Input/Output Channel 2 Digital 7 Green Output (MSB)
111		OSDR1 DRO2_0	IN/OUT	LV	Graphic Red 1 Input/Output Channel 2 Digital 0 Red Output (LSB)
112		OSDR0 DRO2_1	IN/OUT	LV	Graphic Red 0 Input/Output (LSB) Channel 2 Digital 1 Red Output
113		GND3.3IO1	SUPPLY	OBL	Ground Digital Input/Output Port 1
114		VSUP3.3IO1	SUPPLY	OBL	Supply Voltage Input/Output Port 1, 3.3 V
115		PCS5 P2_6	IN/OUT	LV	Flat Panel Control Select 5 PWM Output Port 2, Bit 6 Input/Output
116		PCS4 P2_7	IN/OUT	LV	Flat Panel Control Select 4 REV Output Port 2, Bit 7 Input/Output
117		PCS3 P4_0	IN/OUT	LV	Flat Panel Control Select 3 DE2 Output Port 4, Bit 0 Input/Output
118		PCS2 P4_1	IN/OUT	LV	Flat Panel Control Select 2 DE1 Output Port 4, Bit 1 Input/Output
119		PCS1 P4_2	IN/OUT	LV	Flat Panel Control Select 1 V Output Port 4, Bit 2 Input/Output
120		PCS0 P4_3	IN/OUT	LV	Flat Panel Control Select 0 H Output Port 4, Bit 3 Input/Output
121		PCLK2	OUT	LV	Flat Panel Control Clock 2 Output
122		PCLK1	OUT	LV	Flat Panel Control Clock 1 Output
123		GND1.8DIG	SUPPLY	OBL	Ground Digital Core
124		VSUP1.8DIG	SUPPLY	OBL	Supply Voltage Digital Core, 1.8 V
125		DBO1_0 DRO2_2 LVDSA_4P	OUT	LV	Channel 1 Digital 0 Blue Output[1)] (LSB) Channel 2 Digital 2 Red Output[1)] LVDS Channel 1 bit 4 Positive Output[2)]

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
126		DBO1_1 DRO2_3 LVDSA_4N	OUT	LV	Channel 1 Digital 1 Blue Output[1)] Channel 2 Digital 3 Red Output[1)] LVDS Channel 1 bit 4 Negative Output[2)]
127		DBO1_2 DRO2_4 VSUP3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 2 Blue Output[1)] Channel 2 Digital 4 Red Output[1)] Supply Digital Voltage LVDS[2)] Port, 3.3 V
128		DBO1_3 DRO2_5 LVDSA_3P	OUT	LV	Channel 1 Digital 3 Blue Output[1)] Channel 2 Digital 5 Red Output[1)] LVDS Channel 1 bit 3 Positive Output[2)]
129		DBO1_4 DRO2_6 LVDSA_3N	OUT	LV	Channel 1 Digital 4 Blue Output[1)] Channel 2 Digital 6 Red Output[1)] LVDS Channel 1 bit 3 Negative Output[2)]
130		DBO1_5 DRO2_7 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 5 Blue Output[1)] Channel 2 Digital 7 Red Output[1)] (MSB) Ground Digital LVDS[2)], 3.3 V
131		DBO1_6 DBO1_0 LVDSA_CLKP	OUT	LV	Channel 1 Digital 6 Blue Output[1)] Channel 1 Digital 0 Blue Output[1)] (LSB) LVDS Channel 1 Clock Positive Output[2)]
132		DBO1_7 DBO1_1 LVDSA_CLKN	OUT	LV	Channel 1 Digital 7 Blue Output[1)] Channel 1 Digital 1 Blue Output[1)] LVDS Channel 1 Clock Negative Output[2)]
133		VSUP3.3IO2 VSUP3.3LVDS	SUPPLY	OBL	Supply Digital Output[1)] Port 2 Supply Digital Voltage LVDS[2)], 3.3 V
134		GND3.3IO2 LVDSA_2P	SUPPLY OUT	OBL LV	Ground Voltage Output[1)] Port 2, 3.3 V LVDS Channel 1 bit 2 Positive Output[2)]
135		DBO1_8 DBO1_2 LVDSA_2N	OUT	LV	Channel 1 Digital 8 Blue Output[1)] Channel 1 Digital 2 Blue Output[1)] LVDS Channel 1 bit 2 Negative Output[2)]
136		DBO1_9 DBO1_3 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 9 Blue Output[1)] (MSB) Channel 1 Digital 3 Blue Output[1)] Ground Digital LVDS[2)], 3.3 V
137		DGO1_0 DBO1_4 LVDSA_1P	OUT	LV	Channel 1 Digital 0 Green Output[1)] (LSB) Channel 1 Digital 4 Blue Output[1)] LVDS Channel 1 bit 1 Positive Output[2)]
138		DGO1_1 DBO1_5 LVDSA_1N	OUT	LV	Channel 1 Digital 1 Green Output[1)] Channel 1 Digital 5 Blue Output[1)] LVDS Channel 1 bit 1 Negative Output[2)]
139		DGO1_2 DBO1_6 VSUP3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 2 Green Output[1)] Channel 1 Digital 6 Blue Output[1)] Supply Digital Voltage LVDS[2)], 3.3 V
140		DGO1_3 DBO1_7 LVDSA_0P	OUT	LV	Channel 1 Digital 3 Green Output[1)] Channel 1 Digital 7 Blue Output[1)] (MSB) LVDS Channel 1 bit 0 Positive Output[2)]

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
141		DGO1_4 DGO1_0 LVDSA_0N	OUT	LV	Channel 1 Digital 4 Green Output[1)] Channel 1 Digital 0 Green Output[1)] (LSB) LVDS Channel 1 bit 0 Negative Output[2)]
142		DGO1_5 DGO1_1 VSUP1.8LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 5 Green Output[1)] Channel 1 Digital 1 Green Output[1)] Supply Analog Voltage LVDS[2)], 1.8 V
143		DGO1_6 DGO1_2 REXT	OUT ANA	LV OBL	Channel 1 Digital 6 Green Output[1)] Channel 1 Digital 2 Green Output[1)] LVDS External Resistor[2)]
144		DGO1_7 DGO1_3 GND1.8LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 7 Green Output[1)] Channel 1 Digital 3 Green Output[1)] Ground Analog LVDS[2)], 1.8 V
145		DGO1_8 DGO1_4 LVDSB_3P	OUT	LV	Channel 1 Digital 8 Green Output[1)] Channel 1 Digital 4 Green Output[1)] Dual-LVDS Channel 2 bit 3 Positive Output[2)]
146		DGO1_9 DGO1_5 LVDSB_3N	OUT	LV	Channel 1 Digital 9 Green Output[1)] (MSB) Channel 1 Digital 5 Green Output[1)] Dual-LVDS Channel 2 bit 3 Negative Output[2)]
147		DRO1_0 DGO1_6 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 0 Red Output[1)] (LSB) Channel 1 Digital 6 Green Output[1)] Ground Digital LVDS[2)], 3.3 V
148		DRO1_1 DGO1_7 LVDSBCLKP	OUT	LV	Channel 1 Digital 1 Red Output[1)] Channel 1 Digital 7 Green Output[1)] (MSB) Dual-LVDS Channel 2 Clock Positive Output[2)]
149		GND3.3IO2 LVDSBCLKN	SUPPLY OUT	OBL LV	Ground Digital Output[1)] Port 2 Dual-LVDS Channel 2 Clock Negative Output[2)]
150		VSUP3.3IO2 VSUP3.3LVDS	SUPPLY	OBL	Supply Voltage Output[1)] Port 2, 3.3 V Supply Digital Voltage LVDS[2)], 3.3 V
151		DRO1_2 DRO1_0 LVDSB_2P	OUT	LV	Channel 1 Digital 2 Red Output[1)] Channel 1 Digital 0 Red Output[1)] (LSB) Dual-LVDS Channel 2 bit 2 Positive Output[2)]
152		DRO1_3 DRO1_1 LVDSB_2N	OUT	LV	Channel 1 Digital 3 Red Output[1)] Channel 1 Digital 1 Red Output[1)] Dual-LVDS Channel 2 bit 2 Negative Output[2)]
153		DRO1_4 DRO1_2 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 4 Red Output[1)] Channel 1 Digital 2 Red Output[1)] Ground Digital LVDS[2)], 3.3 V
154		DRO1_5 DRO1_3 LVDSB_1P	OUT	LV	Channel 1 Digital 5 Red Output[1)] Channel 1 Digital 3 Red Output[1)] Dual-LVDS Channel 2 bit 1 Positive Output[2)]
155		DRO1_6 DRO1_4 LVDSB_1N	OUT	LV	Channel 1 Digital 6 Red Output[1)] Channel 1 Digital 4 Red Output[1)] Dual-LVDS Channel 2 bit 1 Negative Output[2)]

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
156		DRO1_7 DRO1_5 VSUP3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 7 Red Output[1)] Channel 1 Digital 5 Red Output[1)] Supply Digital Voltage LVDS[2)], 3.3 V
157		DRO1_8 DRO1_6 LVDSB_0P	OUT	LV	Channel 1 Digital 8 Red Output[1)] Channel 1 Digital 6 Red Output[1)] Dual-LVDS Channel 2 bit 0 Positive Output[2)]
158		DRO1_9 DRO1_7 LVDSB_0N	OUT	LV	Channel 1 Digital 9 Red Output[1)] (MSB) Channel 1 Digital 7 Red Output[1)] (MSB) Dual-LVDS Channel 2 bit 0 Negative Output[2)]
159		P1_7 TDO	IN/OUT	OBL	Port 1, Bit 7 Input/Output JTAG Interface Data Output
160		P1_6 TCLK	IN/OUT	OBL	Port 1, Bit 6 Input/Output JTAG Interface Clock Input
161		P1_5	IN/OUT	LV	Port 1, Bit 5 Input/Output
162		P1_4	IN/OUT	LV	Port 1, Bit 4 Input/Output
163		GND3.3DAC	SUPPLY	OBL	Ground DAC
164		VSUP3.3DAC	SUPPLY	OBL	Supply Voltage DAC, 3.3V
165		P1_3 ROUT	IN/OUT	LV	Port 1, Bit 3 Input/Output Analog Red Output
166		P1_2 GOUT	IN/OUT	LV	Port 1, Bit 2 Input/Output Analog Green Output
167		P1_1 BOUT	IN/OUT	LV	Port 1, Bit 1 Input/Output Analog Blue Output
168		P1_0 SVMOUT	IN/OUT	LV	Port 1, Bit 0 Input/Output Scan Velocity Modulation Output
169		VSUP1.8FE	SUPPLY	OBL	Supply Voltage Analog Video Frontend, 1.8 V
170		VSUP3.3FE	SUPPLY	OBL	Supply Voltage Analog Video Frontend, 3.3 V
171		VIN22 DHS	IN	GND	Analog Video 22 H-Sync Input Digital Video H-Sync Input
172		VIN21	IN	GND	Analog Video 21 B HD Input
173		VIN20	IN	GND	Analog Video 20 G HD Input
174		VIN19	IN	GND	Analog Video 19 R HD Input
175		VIN18	IN	GND	Analog Video 18 Fast Blank 2 Input
176		VIN17	IN	GND	Analog Video 17 B HD Input
177		VIN16	IN	GND	Analog Video 16 G HD Input
178		VIN15	IN	GND	Analog Video 15 R HD Input
179		VIN13	IN	GND	Analog Video 13 B HD Input

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
180		VIN12	IN	GND	Analog Video 12 G HD Input
181		VIN11	IN	GND	Analog Video 11 R HD Input
182		VIN9	IN	GND	Analog Video 9 Y or B SD Input
183		VIN8	IN	GND	Analog Video 8 C or Fast Blank 1 Input
184		VIN7	IN	GND	Analog Video 7 Y or G SD Input
185		VSUP1.8FE	SUPPLY	OBL	Supply Voltage Analog Video Frontend, 1.8 V
186		GNDA	SUPPLY	OBL	Analog Video Frontend, Platform Ground
187		VIN6	IN	GND	Analog Video 6 C or R SD Input
188		VIN5	IN	GND	Analog Video 5 Y/CVBS Input
189		VIN3	IN	GND	Analog Video 3 CVBS Input
190		VIN2	IN	GND	Analog Video 2 CVBS Input
191		VIN1	IN	GND	Analog Video 1 CVBS Input
192		VSUP3.3VO	SUPPLY	OBL	Supply Voltage Analog Video Output, 3.3 V
193		VOUT3	OUT	LV	Analog cvbs Video 3 Output
194		VOUT2	OUT	OBL	Analog cvbs Video 2 Output
195		VOUT1	OUT	OBL	Analog cvbs Video 1 Output
196		GND3.3IO3	SUPPLY	OBL	Ground Digital Input/Output Port 1
197		VSUP3.3IO3	SUPPLY	OBL	Supply Voltage Input/Output Port 1, 3.3 V
198		656I0 P3_0	IN/OUT	LV	Digital 656 Bit 0 Input (LSB) Port 3, Bit 0 Input/Output
199		656I1 P3_1	IN/OUT	LV	Digital 656 Bit 1 Input Port 3, Bit 1 Input/Output
200		656I2 P3_2	IN/OUT	LV	Digital 656 Bit 2 Input Port 3, Bit 2 Input/Output
201		656I3 P3_3	IN/OUT	LV	Digital 656 Bit 3 Input Port 3, Bit 3 Input/Output
202		656I4 P3_4	IN/OUT	LV	Digital 656 Bit 4 Input Port 3, Bit 4 Input/Output
203		656I5 P3_5	IN/OUT	LV	Digital 656 Bit 5 Input Port 3, Bit 5 Input/Output
204		656I6 P3_6	IN/OUT	LV	Digital 656 Bit 6 Input Port 3, Bit 6 Input/Output
205		656I7 P3_7	IN/OUT	LV	Digital 656 Bit 7 Input Port 3, Bit 7 Input/Output
206		656CLKI	IN/OUT	GND	Digital 656 Clock Input

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
207		656CLKO	OUT	LV	Digital 656 Clock Output
208		656O7 P4_7 TCLKFW	IN/OUT	LV	Digital 656 Bit 7 Output Port 4, Bit 7 Input/Output JTAG Interface Clock Input (firmw. Controler)

1) only in RGB output version
2) only in LVDS output version

Display	CRT								FPD											
Application	Analog RGB + SVMOUT + H + V								TTL (Single RGB), LVDS (Dual or Single)								TTL (Dual RGB)			
Panel control									X	X	X	X	X	X	X	X	X	X	X	X
656IN	X	X	X		X	X			X	X	X		X	X			X		X	
656OUT	X	X	X	X					X	X	X	X					X	X		
OSD444	X			X	X		X		X			X	X		X					
OSD222		X				X				X				X						
Port 1	4	4	4	4	4	4	4	4	8	8	8	8	8	8	8	8	8	8	8	8
Port 2	8	8	8	8	8	8	8	8	6	6	6	6	6	6	6	6	6	6	6	6
Port 3		6	8	8		6	8	8		6	6	8		6	8	8		8		8
Port 4	2	2	2	2	8	8	8	8					8	8	8	8			8	8
Max Number of Ports	14	20	22	22	20	26	28	28	14	20	20	22	22	28	30	30	14	22	22	30

Note: 24bit RGB input is always available

Maximum Number of Ports

2.2.2. Pin Descriptions

2.2.2.1. Supply Pins

VSUP1.8DIG – Supply Voltage 1.8 V
This pin is main and standby supply for the digital core logic of controller, video and display processing.

VSUP1.8FE – Supply Voltage 1.8 V
This pin is main and standby supply for the analog video frontend.

VSUP3.3FE – Supply Voltage 3.3 V
This pin is main and standby supply for the analog video frontend.

VSUP3.3VO – Supply Voltage 3.3 V
This pin is main and standby supply for the analog video outputs.

VSUP1.8LVDS – Supply Voltage 1.8 V
This pin is main and standby supply for the analog LVDS core.

VSUP3.3LVDS – Supply Voltage 3.3 V
This pin is main and standby supply for the Digital LVDS port.

VSUP3.3FL – Supply Voltage 3.3 V
This pin is main and standby supply for the Flash device.

VSUP3.3DRI – Supply Voltage 3.3 V
This pin is main supply for the digital RAM interface.

VSUP3.3RAM – Supply Voltage 3.3 V
This pin is main supply for the RAM device

VSUP3.3IO 1-3 – Supply Voltage 3.3 V
This 3 pins are main and standby supply for the digital I/O-ports.

VSUP3.3COM – Supply Voltage 3.3 V
This pin is main and standby supply for the digital Input ports and common digital logic.

VSUP3.3DIG – Supply Voltage 3.3 V
This pin is main supply for the digital core logic of IF and audio processing and digital video backend.

VSUP8.0AU – Supply Voltage 8.0 V
This pin is main supply for the analog audio processing.

VSUP5.0SIF – Supply Voltage 5.0 V
This pin is main supply for the SIF processing.

VSUP3.3DAC – Supply Voltage 3.3 V
This pin is main and standby supply for the Analog DAC.

GND* – Ground
This pin are main ground for all digital analog and port supplies.

Application Note:

All GND pins must be connected to a low-resistive ground plane underneath the IC. All supply pins must be connected separately with short and low-resistive lines to the power supply. Decoupling capacitors from VSUPxx to GND have to be placed as closely as possible to these pins. It is recommended to use more than one capacitor. By choosing different values, the frequency range of active decoupling can be extended.

2.2.2.2 Audio Pins

VREFAU – Reference Voltage for Analog Audio
This pin serves as the internal ground connection for the analog audio circuitry. It must be connected to the **GND** pin with a 3.3 µF and a 100 nF capacitor in parallel.

SGND – Analog Reference Input
This is the reference ground Analog Audio part.

AIN1 R/L – Audio 1 Inputs
The analog input signal for audio 1 is fed to this pin. Analog input connection must be AC coupled.

AIN2 R/L – Audio 2 Inputs
The analog input signal for audio 2 is fed to this pin. Analog input connection must be AC coupled.

AIN3 R/L – Audio 3 Inputs
The analog input signal for audio 3 is fed to this pin. Analog input connection must be AC coupled.

AIN4 R/L – Audio 4 Inputs
The analog input signal for audio 4 is fed to this pin. Analog input connection must be AC coupled.

AIN5 R/L – Audio 5 Inputs
The analog input signal for audio 5 is fed to this pin. Analog input connection must be AC coupled.

AOUT1 R/L – Audio 1 Outputs
Output of the analog audio 1 signal. Connections to these pins are intended to be AC coupled.

AOUT2 R/L – Audio 2 Outputs
Output of the analog audio 2 signal. Connections to these pins are intended to be AC coupled.

SPEAKER R/L – Loudspeaker Outputs
Output of the loudspeaker signal.

HEADPHONES R/L – Headphones Outputs
Output of the headphones signal.

2.2.2. Pin Descriptions (Continued)

SUBWOOFER – Subwoofer Outputs
Output of the subwoofer signal

I2S_DEL_WS - Delay Line Bus Word Strobe
This is the word strobe signal of the delay line bus.

I2S_DEL_CL - Delay Line Bus Clock
This is the Clock signal of the delay line bus.

I2S_DEL_IN - Delay Line Bus Data Input
This is the data input signal of the delay line bus.

I2S_DEL_OUT - Delay Line Bus Data Output
This is the data output signal of the delay line bus.

I2S_WS - I2S Word Strobe
This is the word strobe signal of I2S bus.

I2S_DA_IN - I2S Data Input
This is the data input signal of I2S bus.

I2S_CL - I2S Clock
This is the Clock signal of I2S bus.

SPDIF_OUT -
This is an SPDIF output signal to connect to an A/V receiver.

SIF –/+ – Sound IF Input
This is the SIF input to connect to an external DRX.

VREFSIF – Reference Voltage for SIF
This pin serves as the internal ground connection for the analog audio circuitry.

2.2.2.3 Video Pins

656I 0-7 – Digital 656 Data Input
These are the 8 bits digital 656 video inputs.

656CLKI – Digital 656 Input clock
This is the clock for the digital 656 video inputs.

656O 0-7 – Digital 656 Data Output
These are the 8 bits digital 656 video outputs.

656CLKO– Digital 656 output clock
This is the clock for the digital 656 video outputs.

OSDR 0-3 – Graphic Data input/output
These are the 2 or 4 bit graphic input/output

OSDG 0-3 – Graphic Data input/output
These are the 2 or 4 bit graphic input/output

OSDB 0-3 – Graphic Data input/output
These are the 2 or 4 bit graphic input/output

OSDHCS 0-1 – Graphic Half Contrast Input/Output
This is the half contrast for the graphic input/output

OSDFSW – Graphic Fast Switch Input/Output
This is the fast switch for the graphic input/output

OSDCLK – Graphic clock Input/Output
This is the clock for the graphic video input/output

OSDV – Graphic vertical sync Input/Output
This is the vertical sync for the graphic input/output

OSDH – Graphic horizontal sync Input/Output
This is the horizontal sync signal for the graphic I/O

DRO1_ 0-9 - Digital Red Outputs
This are 10 bits digital signals for red outputs, for dual RGB use bits (0-7).

DGO1_ 0-9 - Digital Green Output
This are 10 bits digital signals for green outputs, for dual RGB use bits (0-7).

DBO1_ 0-9 - Digital Blue Outputs
This are 10 bits digital signals for blue outputs, for dual RGB use bits (0-7).

DRO2_ 0-7 - Digital dual Red Outputs
This are 8 bits digital signals for red outputs.

DGO2_ 0-7 - Digital dual Green Output
This are 8 bits digital signals for green outputs.

DBO2_ 0-7 - Digital dual Blue Outputs
This are 8 bits digital signals for blue outputs.

PCS 0-5 - LCD Panel Control Select Outputs
This are 6 control select signals for LCD outputs.
For CRT application use PCS_0 as H sync and PCS_1 as V sync Back End.

PCLK1,2 - LCD Panel Clock Outputs
This are the clock signals for LCD/RGB outputs.

LVDSA_* - LCD Panel LVDS Outputs
This are 12 signals and clocks for LVDS single or dual output.

LVDSB_* - LCD Panel LVDS Outputs
This are 10 signals and clocks for LVDS dual output.

REXT - LVDS External Resistor
This pin is connected to the external LVDS resistor. (6.2 kOhm to gnd)

DRI 0-7 - Digital video inputs for Red
This are 8 bits digital inputs for red signal

DGI 0-7- Digital video inputs for Green
This are 8 bits digital inputs for green signal

DBI 0-7- Digital video inputs for Blue
This are 8 bits digital inputs for blue signal.

DEN - Digital video inputs Enable
This is the enable signal for the Digital Video Inputs.

DHS - Digital video inputs Horizontal Sync
This is the H Sync signal for the Digital RGB input bus or for the VGA Video Inputs.

DVS - Digital video inputs Vertical Sync
This is the V Sync signal for the Digital RGB input bus or for the VGA Video Inputs.

DCLK - Digital video inputs Clock
This is the Clock signal for the Digital Video Inputs.

CLKOUT – Digital Output clock
This is a 20MHz clock for the external video ICs.

VIN 1–22 – Analog Video Input
These are the 19 analog video inputs.
(Vin 4,10 and 14 are missing)
A CVBS, S-VHS, YCrCb or RGB signal is converted using the luma, chroma and component AD converter.
Vin 8,18 are fast blank inputs. Vin22 is an Hsync input.
The input signals must be AC-coupled.

VOUT 1-3 – Analog Video Output
The analog video inputs that are selected by the video matrix are output at these pins.

ROUT, GOUT, BOUT – Analog RGB Output
These pins are the analog Red/Green/Blue outputs of the back-end.

SVMOUT – Scan Velocity Modulation Output
This output delivers the analog SVM signal. The D/A converter is a current sink like the RGB D/A converters. At zero signal the output current is 50% of the maximum output current.

2.2.2.4 Controller Pins

XTALIN Crystal Input and **XTALOUT** Crystal Output
These pins are connected to an 20.25 MHz crystal oscillator. An external clock can be fed into XTALIN.

RESETQ – Reset Input/Output
A low level on this pin resets the VCT 69xyP. The internal CPU can pull down this pin to reset external devices connected to this pin.

TEST – Test Input
This pin enables factory test modes. For normal operation, it must be connected to ground.

SCL – I^2C Bus Clock
This pin delivers the I^2C bus clock line. The signal can be pulled down by external slave ICs to slow down data transfer.

SDA – I^2C Bus Data
This pin delivers the I^2C bus data line.

P1_0–**P1_3** – I/O Port
These pins provide CPU controlled I/O ports.

P1_4–**P1_7** – I/O Port
These pins provide CPU controlled I/O ports.
Also used as **CADC1**–**4** – Controller A/D inputs 1 to 4.
This 4 pins are analog/digital converters from the controller

P2_0–**P2_7** – I/O Port
These pins provide CPU controlled I/O ports.

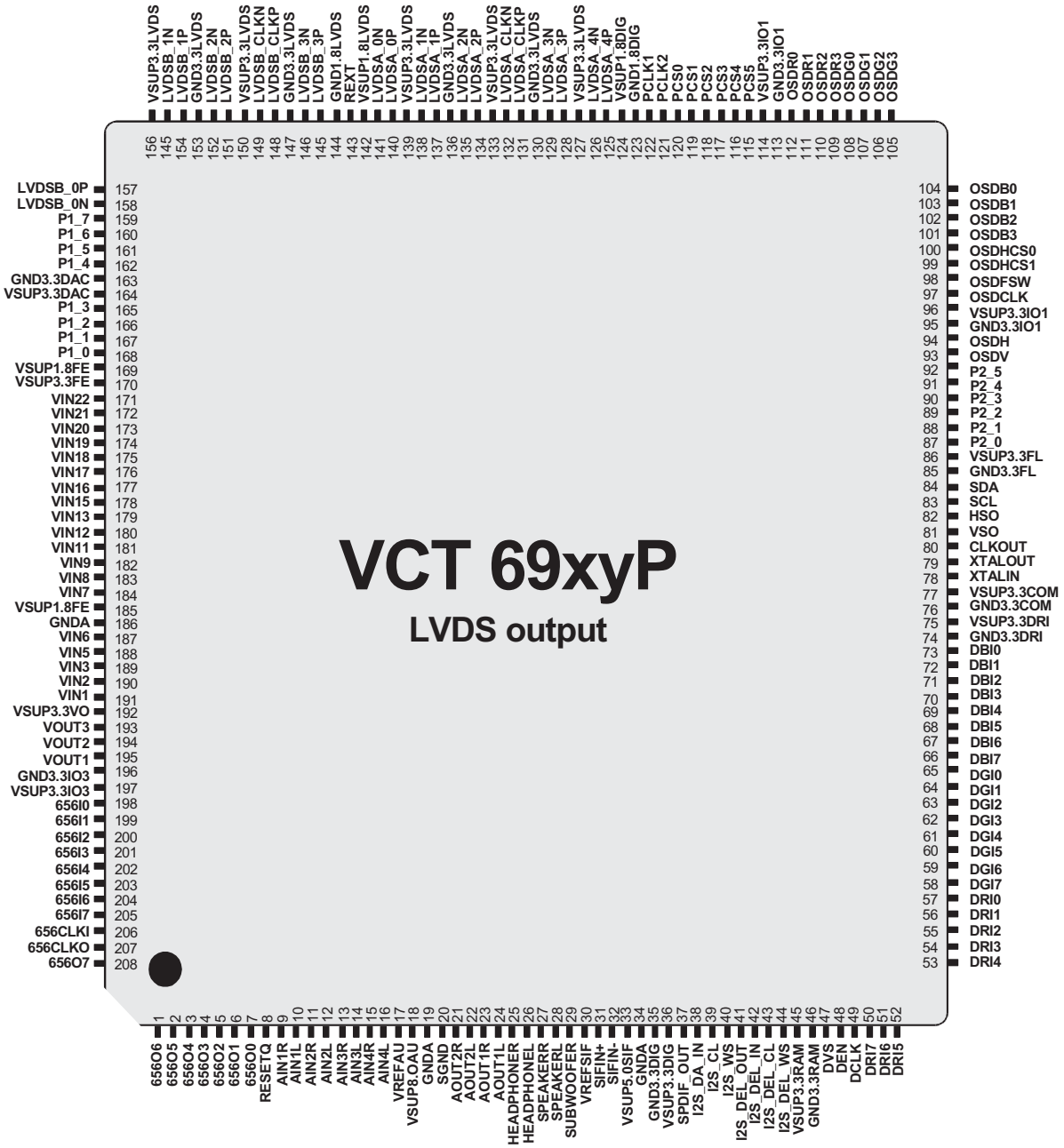
P3_0–**P3_7** – I/O Port
These pins provide CPU controlled I/O ports.

P4_0–**P4_7** – I/O Port
These pins provide CPU controlled I/O ports.

TDO-TCLK-TDI-TMS -JTAG Interface Pins for TV controler.
TCLK at pin 4 (656O3) has during reset an internal pull up: (TCLK=0) at end of reset enables the JTAG mode at 656 LSB's, this can also be done via I2C.
This JTAG is also available at Port(1 and 2) but only via I2C.

TDOFW-TCLKFW-TDIFW-TMSFW -JTAG Interface Pins for firmware controler.
TCLKFW at pin 208 (656O7) has during reset an internal pull up: (TCLKFW=0) at end of reset enables the JTAG mode, this can also be done via I2C.

2.2.3. Pinning



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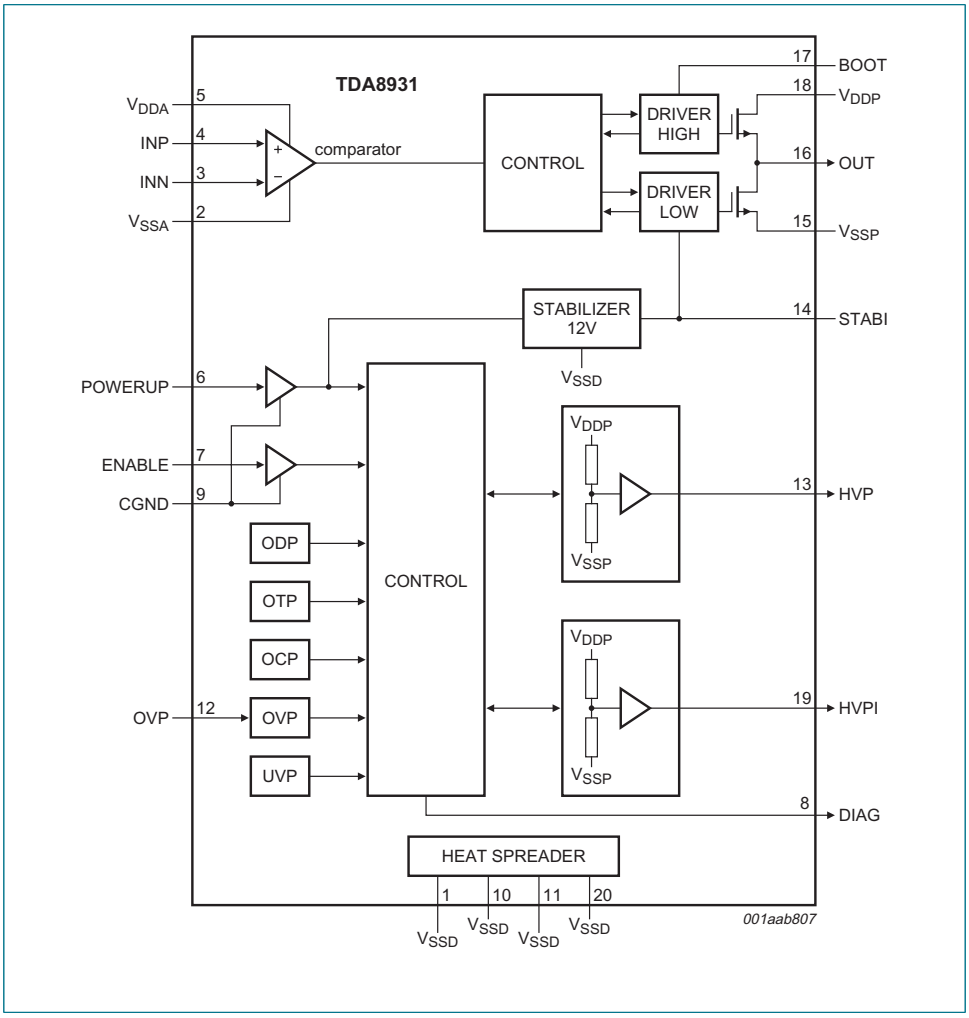
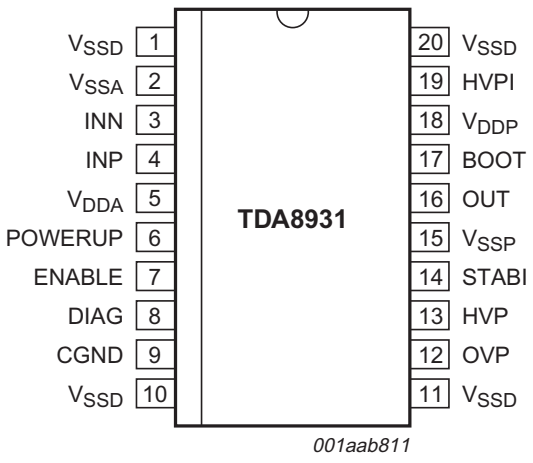
2.3. IC301, IC302 (VHITDA8931T-1Y)

2.3.1. Block Diagram

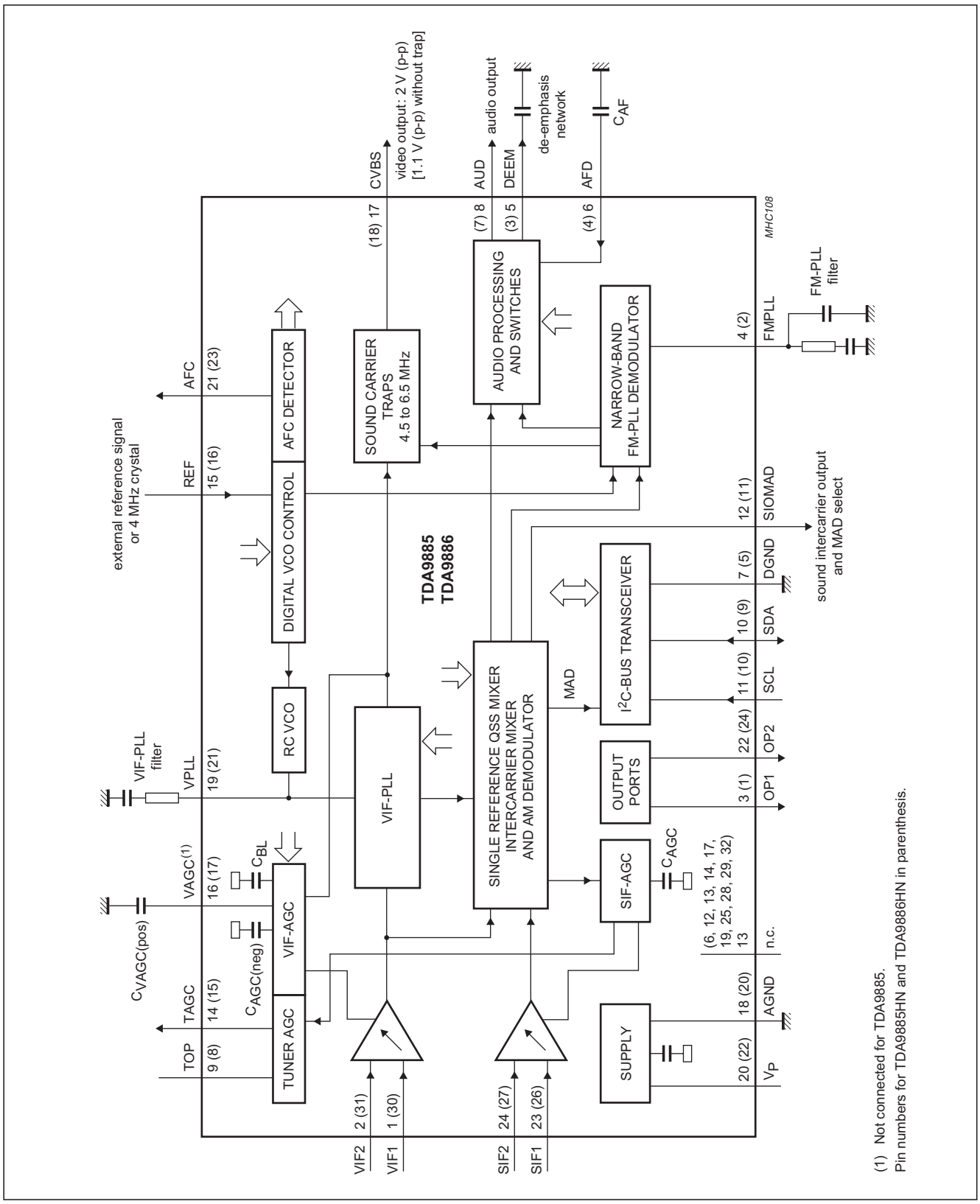


2.3.2. Pinning



2.4. IC201 (VHITDA9886+-1Y)

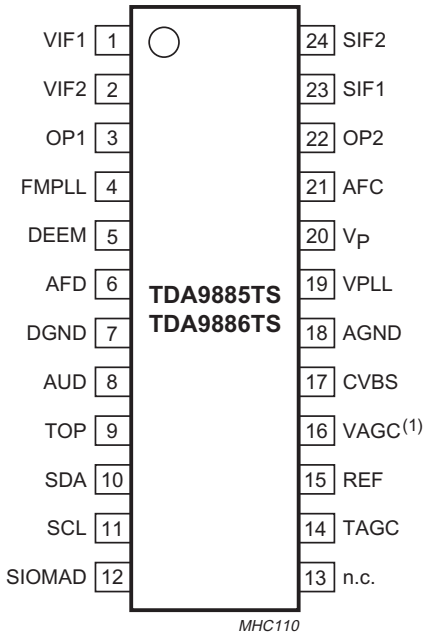
2.4.1. Block Diagram



2.4.2. Pinning

SYMBOL	PIN				DESCRIPTION
	TDA9885T TDA9885TS	TDA9886T TDA9886TS	TDA9885HN	TDA9886HN	
VIF1	1	1	30	30	VIF differential input 1
VIF2	2	2	31	31	VIF differential input 2
n.c.	–	–	32	32	not connected
OP1	3	3	1	1	output port 1; open-collector
FMPLL	4	4	2	2	FM-PLL for loop filter
DEEM	5	5	3	3	de-emphasis output for capacitor
AFD	6	6	4	4	AF decoupling input for capacitor
DGND	7	7	5	5	digital ground
n.c.	–	–	6	6	not connected
AUD	8	8	7	7	audio output
TOP	9	9	8	8	tuner AGC TakeOver Point (TOP) for resistor adjustment
SDA	10	10	9	9	I^2C-bus data input and output
SCL	11	11	10	10	I^2C-bus clock input
SIOMAD	12	12	11	11	sound intercarrier output and MAD select with resistor
n.c.	–	–	12	12	not connected
n.c.	13	13	13	13	not connected
n.c.	–	–	14	14	not connected
TAGC	14	14	15	15	tuner AGC output
REF	15	15	16	16	4 MHz crystal or reference signal input
VAGC	–	16	–	17	VIF-AGC for capacitor
n.c.	16	–	17	–	not connected
CVBS	17	17	18	18	composite video output
n.c.	–	–	19	19	not connected
AGND	18	18	20	20	analog ground
VPLL	19	19	21	21	VIF-PLL for loop filter
V_P	20	20	22	22	supply voltage
AFC	21	21	23	23	AFC output
OP2	22	22	24	24	output port 2; open-collector
n.c.	–	–	25	25	not connected
SIF1	23	23	26	26	SIF differential input 1 and MAD select with resistor
SIF2	24	24	27	27	SIF differential input 2 and MAD select with resistor
n.c.	–	–	28	28	not connected
n.c.	–	–	29	29	not connected

2.4.2. Pinning (Continued)

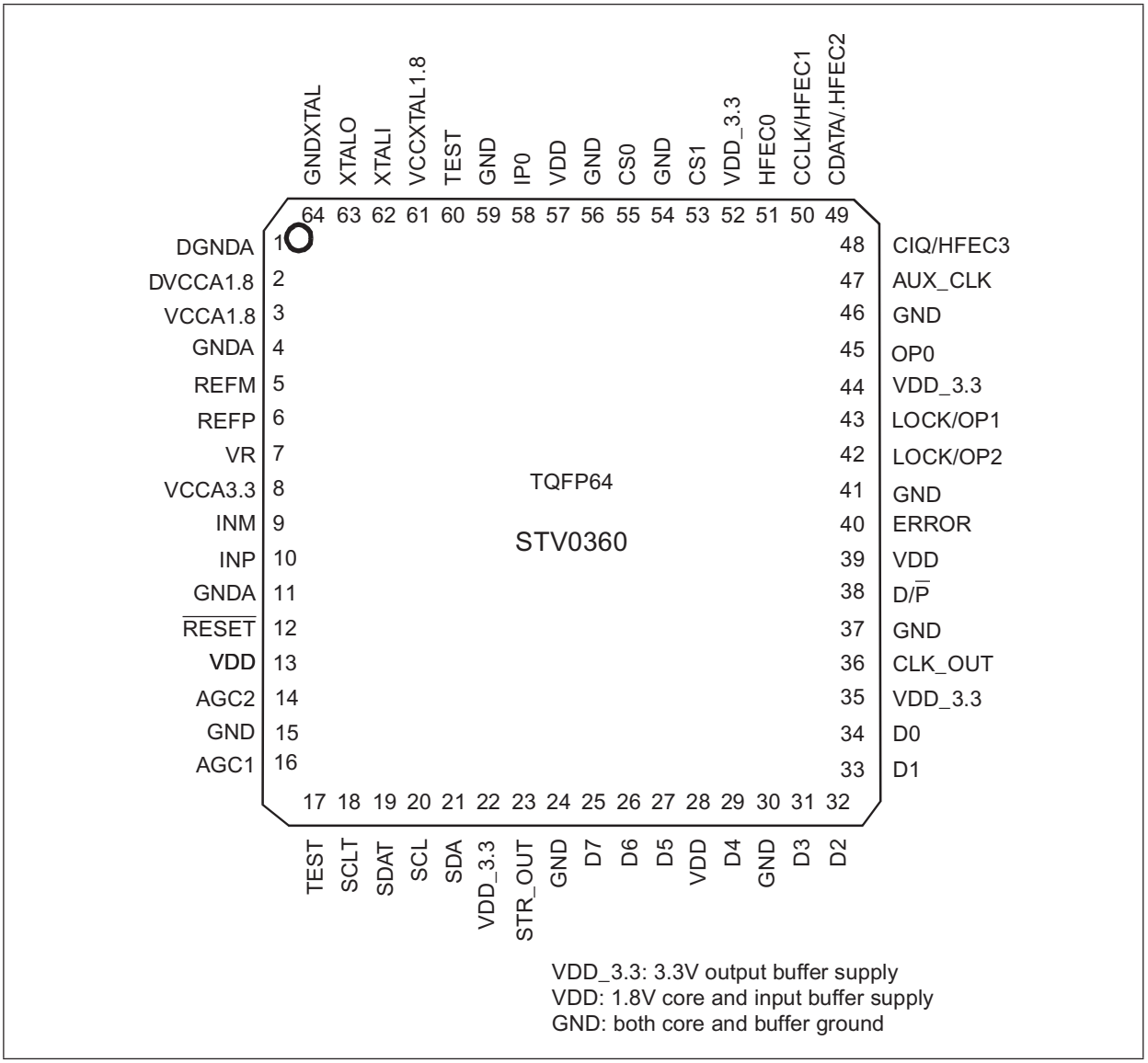


(1) Not connected for TDA9885TS.

Fig.3 Pin configuration for SSOP24.

2.5. IC202 (STV0360)

2.5.1. Pinning



2.5.2. Pin Description

Pin number	Name	Type	Description	Drive (mA)
Clock and resets				
12	$\overline{\text{RESET}}$	I[1]	Hardware reset, active low	-
62	XTALI	Analog	Crystal oscillator input/external clock (1.8 V)	-
63	XTALO	Analog	Crystal oscillator output	-
61	VCCXTAL1.8	Supply	Analog oscillator supply (1.8 V)	-
64	GNDXTAL	Ground	Analog oscillator ground	-
Analog interface				
2	DVCCA1.8	Supply	Analog part digital supply (1.8 V)	-
5	REFM	Analog	Internal negative reference	-
6	REFP	Analog	Internal positive reference	
3	VCCA1.8	Supply	Analog supply (1.8 V)	-
9	INM	Analog	Negative analog input	-
10	INP	Analog	Positive analog input	-
4, 11	GNDA	Supply	Analog ground	-
1	DGNDA	Ground	Analog ground	-
7	VR	Analog	Reference	-
8	VCCA3.3	Supply	Analog supply (3.3 V)	
I^2C interface				
21	SDA	IO[2]	Serial data (open drain)	8
20	SCL	I	Serial clock (open drain)	-
19	SDAT	IO	SDA tuner (open drain)	4
18	SCLT	I	SCL tuner	
MPEG interface				
25, 26, 27, 29, 31, 32, 33, 34	D7/0	O[3]	Serial D7, MPEG data	8/4
36	CLK_OUT	O	MPEG byte or bit clock	4
23	STR_OUT	O	MPEG first byte sync	2
38	D/$\overline{\text{P}}$	O	MPEG data valid/parity	4
40	ERROR	O	MPEG packet error	2
51	HFEC0	O	Hierarchical FEC output bit 0	2
50	CCLK/HFEC1	O	Hierarchical FEC output bit 1 or clock for constellation display	2
49	CDATA/HFEC2	O	Hierarchical FEC output bit 2 or data for constellation display	2
48	CIQ/HFEC3	O	Hierarchical FEC output bit 3 or IQ validation for constellation display	2

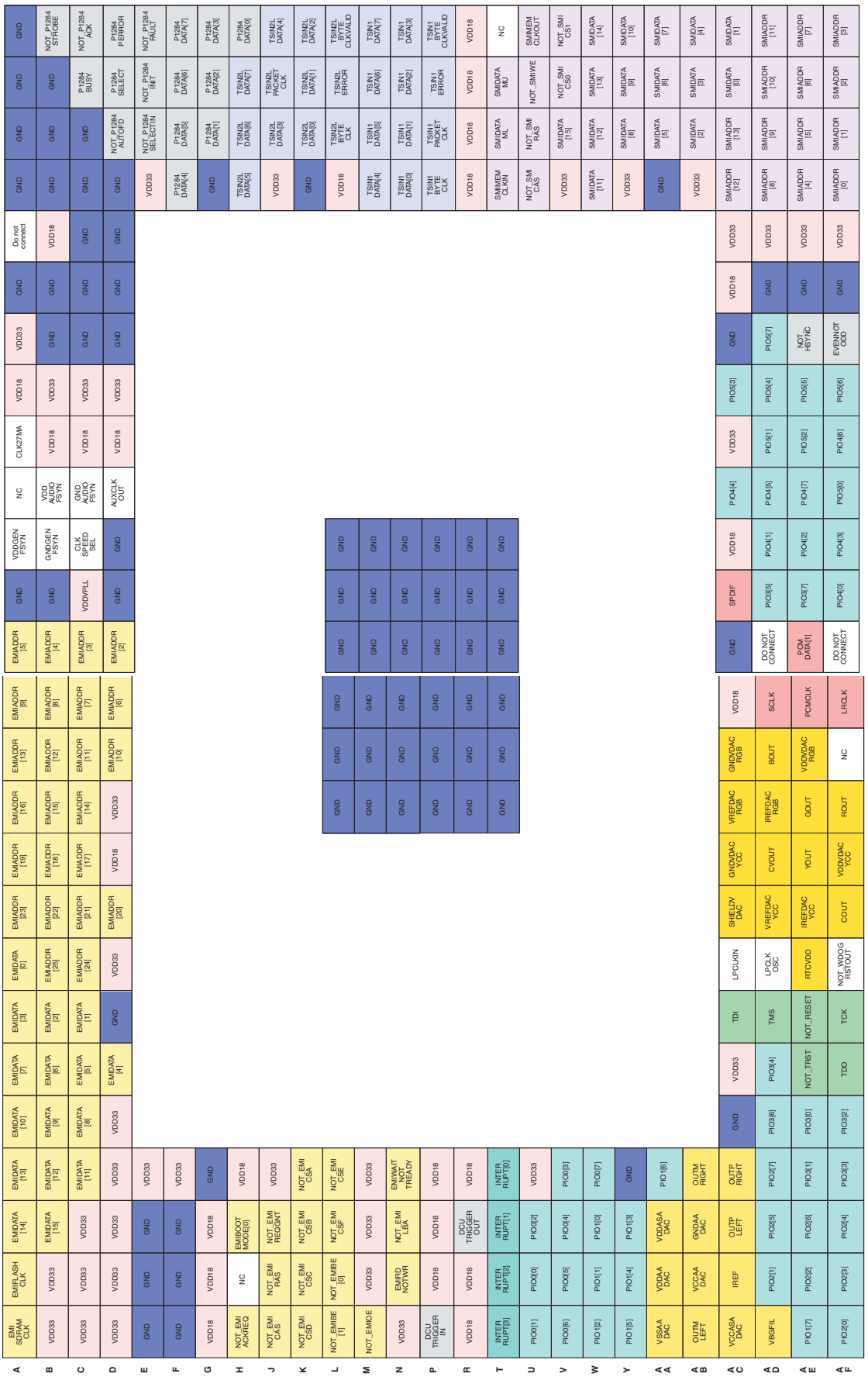
2.5.2. Pin Description (Continued)

Pin number	Name	Type	Description	Drive (mA)
Front end controls				
16	AGC1	IO	RF AGC control ΣΔ	4
14	AGC2	IO	IF AGC control ΣΔ	4
17, 60	TEST		Reserved test mode, must be grounded	
58	IP0	I	General-purpose input port 0 and ADC input for RF level monitoring	-
45	OP0	IO	General-purpose output port 0	4
43	LOCK/OP1	IO	General-purpose output port 1 or lock indicator	4
42	LOCK/OP2	O	General-purpose output port 2 or lock indicator	4
47	AUX_CLK	IO	Auxiliary clock	8
55	CS0	I	Chip select LSB	-
53	CS1	I	Chip select MSB	-
Power supply				
13, 28, 39, 57	VDD	Supply	Digital core supply	
22, 35, 44, 52	VDD_3.3	Supply	Digital IO supply	
15, 24, 30, 37, 41, 46, 54, 56, 59	GND	Ground		

1. All inputs are 3.3 V compatible
2. All bidirectional pads are 3.3 V capable
3. All outputs are 3.3 V capable

2.6. IC4001 (Sti5516)

2.6.1. Pinning



2.6.2. Pin Description

STi5516 pin list

Signal names are prefixed by NOT_ if they are active low; otherwise they are active high.
All signals are only 3.3 V capable unless otherwise indicated as 1.8 V or 5 V tolerant.

Table 2: I/O load capacitance and DC loading

Pad type	Functional pin group	Maximum load capacitance (pF)	Drive (mA)	Notes
C4	Others	75	4	
S8	SDRAM/EMI	75	8	
S8b	SDRAM/EMI	75	8	
E8	EMI (programmable)	35	8	a
		25	6	a
		15	4	a
		5	2	a
P4	PIO	400	4	

a. Typical load, but the maximum is 75 pF

Table 3: Analog power supply pins

Pin	Location	Number	Function
VDDVDACRGB	AE12	1	3.3 V power supply for RGB video DAC
VDDVDACYCC	AF10	1	3.3 V power supply for YCC video DAC
GNDVDACRGB	AC12	1	Ground for RGB video DAC
GNDVDACYCC	AC10	1	Ground for YCC video DAC
SHIELDVDAC	AC9	1	Shield ground for 2 x video DACs
IREFDACRGB	AD11	1	RGB video DAC current reference
IREFDACYCC	AE9	1	YCC video DAC current reference
VREFDACRGB	AC11	1	RGB video DAC voltage reference
VREFDACYCC	AD9	1	YCC video DAC voltage reference
VDDVPLL	C15	1	3.3 V power for video PLL
VDDAUDIOFSYN	B17	1	1.8 V dedicated power for low jitter audio clock frequency synthesizer
GNDAUDIOFSYN	C17	1	Dedicated ground for low jitter audio clock frequency synthesizer
VDDGENFSYN	A16	1	1.8 V dedicated power for nonaudio clock frequency synthesizer
GNDGENFSYN	B16	1	Dedicated ground for nonaudio clock frequency synthesizer
VDDAADAC	AA2	1	3.3 V power for audio DAC
VSSAADAC	AA1	1	Ground for audio DAC command switches

2.6.2. Pin Description (Continued)

Table 3: Analog power supply pins

Pin	Location	Number	Function
VDDASADAC	AA3	1	3.3 V power for audio DAC substrate
VCCAADAC	AB2	1	3.3 V power for audio DAC command switches
GNDAADAC	AB3	1	Ground for audio DAC
VCCASADAC	AC1	1	3.3 V power for audio DAC command switches substrate
IREF	AC2	1	Audio DAC output reference current
VBGFIL	AD1	1	Audio DAC filtered output reference voltage

Table 4: Digital power supply pins

Pin	Location	Number	Function
VDD18	a	24	1.8 V power supply
VDD33	b	35	3.3 V power supply
RTCVDD	AE8	1	Low power controller 1.8 V power supply
GND	c	76	Ground for power supplies

a. A19, B18, B22, C18, D10, D18, G1 to G3, H4, L23, P2 to P4, R1, R2, R4, R23 to R26, AC13, AC16 and AC21.

b. A20, B1, B2, B19, C1 to C3, C19, D1 to D5, D8, D11, D19, E4, E23, F4, J4, J23, M2 to M4, N1, U4, V23, Y23, AB23, AC6, AC18, AC22, AD22, AE22 and AF22.

c. A15, A21, A23 to A26, B15, B20, B21, B23 to B25, C20 to C24, D7, D15, D16, D20 to D23, E1 to E3, F1 to F3, G4, G23, K23, L11 to L16, M11 to M16, N11 to N16, P11 to P16, R11 to R16, T11 to T16, Y4, AA23, AC5, AC14, AC20, AD21, AE21 and AF21.

Table 5: RTC pins

Pin	Location	I/O	Function
LPCLKIN[a]	AC8	I	Low power clock input
LPCLKOSC[A]	AD8	I/O	Low power clock oscillator

a. 1.8 V tolerant

2.6.2. Pin Description (Continued)

Table 6: System pins

Pin	Location	I/O	Function	Pad type
CLK27MA[A]	A18	I	Selectable input clock to PLL or for x1 mode	C4
CLKSPEEDSEL[a]	C16	I	PLL speed select	C4
AUXCLKOUT[a]	D17	O	Auxiliary clock for general use	C4
NOT_RESET[B]	AE7	I	System reset	-
NOT_WDOGRSTOUT[a]	AF8	O	Internal watchdog timer reset.	C4

a. 5 V tolerant
b. 1.8 V tolerant

Table 7: JTAG pins

Pin	Location	I/O	Function	Pad type
TDI[A]	AC7	I	Boundary scan test data input	C4
TMS[a]	AD7	I	Boundary scan test mode select	C4
TCK[a]	AF7	I	Boundary scan test clock	-
NOT_TRST[a]	AE6	I	Boundary scan test logic reset	C4
TDO[a]	AF6	O	Boundary scan test data output	C4

a. 5 V tolerant

Table 8: DCU pins

Pin	Location	I/O	Function	Pad type
DCUTRIGGERIN[a]	P1	I	External trigger input to DCU	C4
DCUTRIGGEROUT[A]	R3	O	Signal to trigger external debug circuitry	C4

a. 5 V tolerant

2.6.2. Pin Description (Continued)

Table 9: EMI pins

Pin	Location	I/O	Function	Pad type
NOT_EMIRAS or NOT_CI_IORD[a]	J2	O	Row address strobe for SDRAM	C4
NOT_EMICAS or NOT_CI_IOW[a]	J1	O	Column address strobe for SDRAM	E8
NOT_EMICSA	K4	O	Peripheral chip select A	E8
NOT_EMICSB	K3	O	Peripheral chip select B	E8
NOT_EMICSC	K2	O	Peripheral chip select C	E8
NOT_EMICSD	K1	O	Peripheral chip select D	E8
NOT_EMICSE	L4	O	Peripheral chip select E	E8
NOT_EMICSF	L3	O	Peripheral chip select F	E8
NOT_EMIBE[1:0]	L1, L2	O	External device data bus byte enable. 1 bit per byte of the data bus.	E8
NOT_EMIOE or NOT_CI_OE	M1	O	External device output enable.	E8
NOT_EMILBA or NOT_CI_WEA	N3	O	Flash device load burst address.	E8
EMIWAITNOTTREADY[b]	N4	I	External memory device target ready indicator	C4
EMIRDNOTWR	N2	O	External read/write access indicator. Common to all devices.	E8
EMIDATA[15:0]	c	I/O	External common data bus.	E8
EMIADDR[25:2][d]	e	O	External common address bus	E8
NOT_EMIREQGNT	J3	O	Bus request/grant indicator	E8
NOT_EMIACKREQ[b]	H1	I	Bus grant/request indicator	C4
EMIBOOTMODE0[b]	H3	I	External power-up port size indicator	C4
EMISDRAMCLK	A1	O	SDRAM clock	E8
EMIFLASHCLK	A2	O	Peripheral clock	E8

a. Or equivalent ATA HDD interface signal.

b. 5 V tolerant

c. B3, A3, A4, B4, C4, A5, B5, C5, A6, B6, C6, D6, A7, B7, C7 and A8.

d. EMIADDR[19:20] are used as ATA HDD interface function: ATA CS0 and CS1. There is no interconnect configuration control register bit to select this function. The addresses are just reused as chip selects.

e. B8, C8, A9, B9, C9, D9, A10, B10, C10, A11, B11, C11, A12, B12, C12, D12, A13, B13, C13, D13, A14, B14, C14 and D14.

2.6.2. Pin Description (Continued)

Table 10: Transport stream 2 pins

Pin	Location	I/O	Function	Pad type
TSIN2LBYTECLK[a]	L24	I/O	Transport stream bit clock	C4
TSIN2LBYTECLKVALID[a]	L26	I/O	Transport stream bit clock valid edge	C4
TSIN2LERROR[a]	L25	I/O	Transport stream packet error	C4
TSIN2LPACKETCLK[a]	J25	I/O	Transport stream packet strobe	C4
TSIN2LDATA[7:0][a]	b c	I/O	Transport stream data	C4

a. 5 V tolerant
b. H25, H24, H23, J26, J24, K26, K25 and K24
c. TSIN2LDATA7 is used for data input in serial mode.

Table 11: Transport stream 1 pins

Pin	Location	I/O	Function	Pad type
TSIN1BYTECLK[a]	P23	I	Transport stream bit/byte clock	C4
TSIN1BYTECLKVALID[a]	P26	I	Transport stream bit/byte clock valid edge	C4
TSIN1ERROR[a]	P25	I	Transport stream packet error	C4
TSIN1PACKETCLK[a]	P24	I	Transport stream packet strobe	C4
TSIN1DATA[7:0][a]	b, c	I	Transport stream data in	C4

a. 5 V tolerant
b. M26, M25, M24, M23, N26, N25, N24 and N23.
c. TSIN1DATA7 is used for data input in serial mode.

2.6.2. Pin Description (Continued)

Table 12: Programmable I/O pins

Pin	Location	I/O	Function	Pad type
PIO0[0:7][A]	b	I/O	Parallel input/output pin or alternative function	P4
PIO1[0:7][a]	c	I/O		P4
PIO2[0:7][a]	d	I/O		P4
PIO3[0:7][a]	e	I/O		P4
PIO4[0:7][a]	f	I/O		P4
PIO5[0:7][a]	g	I/O		P4

a. 5 V tolerant
b. U2, U1, U3, V4, V3, V2, V1 and W4
c. W3, W2, W1, Y3, Y2, Y1, AA4 and AE1
d. AF1, AD2, AE2, AF2, AF3, AD3, AE3 and AD4
e. AE5, AE4, AF5, AF4, AD6, AD15, AD5 and AE15
f. AF15, AD16, AE16, AF16, AC17, AD17, AF18 and AE17
g. AF17, AD18, AE18, AC19, AD19, AE19, AF19 and AD20

Table 13: Digital audio pins[a]

Pin	Location	I/O	Function	Pad type
SCLK[B]	AD13	O	Serial clock	C4
PCMDATA[1][b]	AE14	O	PCM data out	C4
PCMCLK[b]	AE13	I/O	External PCM clock input or internal PCM clock output	C4
LRCLK[b]	AF13	O	Left/right clock	C4
SPDIF[b]	AC15	O	Digital audio output	C4

a. Note: Digital audio input pins PCMI_SCLK, PCMI_DATA and PCMI_LRCLK are alternate functions for NOT_CD_REQ[1], I1284HOSTLOGICHIGH, and NOT_CD_REQ[0], on PIO port 3 bits [6:4]
b. 5 V tolerant

2.6.2. Pin Description (Continued)

Table 14: AVSDRAM pins (SMI)

Pin	Location	I/O	Function	Pad type
SMIADDR[13:0]	a	O	Audio/video core SDRAM address bus	S8
SMIDATA[15:0]	b	I/O	Audio/video core SDRAM data bus	S8
NOT_SMICS0	V25	O	Audio/video core SDRAM chip select for 1st SDRAM	S8
NOT_SMICS1	V26	O	Audio/video core SDRAM chip select for 2nd 16 Mbit SDRAM	S8
NOT_SMICAS	U23	O	Audio/video core SDRAM column address strobe	S8
NOT_SMIRAS	U24	O	Audio/video core SDRAM row address strobe	S8
NOT_SMIWE	U25	O	Audio/video core SDRAM write enable	S8
SMIMEMCLKIN	T23	I	Audio/video core SDRAM memory clock input	S8b
SMIMEMCLKOUT	U26	O	Audio/video core SDRAM memory clock output	S8
SMIDATAML	T24	O	Audio/video core SDRAM data bus lower byte enable	S8
SMIDATAMU	T25	O	Audio/video core SDRAM data bus upper byte enable	S8

a. AC24, AC23, AD26, AD25, AD24, AD23, AE26, AE25, AE24, AE23, AF26, AF25, AF24 and AF23.

b. V24, W26, W25, W24, W23, Y26, Y25, Y24, AA26, AA25, AA24, AB26, AB25, AB24, AC26 and AC25.

Table 15: IEEE 1284/1394 pins

Pin	Location	I/O	Function	Pad type
P1284DATA[7:0][A]	b	I/O	1284 data or 1394 AV data	I14
NOT_P1284SELECTIN[a]	E24	I/O	1284 or 1394 AV control signals	I14
NOT_P1284INIT[a]	E25	I/O		I14
NOT_P1284FAULT[a]	E26	I/O		I14
NOT_P1284AUTOFD[a]	D24	I/O		I14
P1284SELECT[a]	D25	I/O		I14
P1284PERROR[a]	D26	I/O		I14
P1284BUSY[a]	C25	I/O		I14
NOT_P1284ACK[a]	C26	I/O		I14
NOT_P1284STROBE[a]	B26	I/O		I14

a. 5 V tolerant

b. F26, F25, F24, F23, G26, G25, G24 and H26.

2.6.3. Pin Description (Continued)

Table 16: Interrupt pins

Pin	Location	I/O	Function	Pad type
INTERRUPT[3:0][A]	[b]	I/O	External interrupts	C4

a. 5 V tolerant
b. T1, T2, T3 and T4.

Table 17: Analog audio DAC (digital-to-analog converter) pins

Pin	Location	I/O	Function
OUTPLEFT	AC3	O	Left channel, differential positive current output
OUTMLEFT	AB1	O	Left channel, differential negative current output
OUTPRIGHT	AC4	O	Right channel, differential positive current output
OUTMRIGHT	AB4	O	Right channel, differential negative current output

Table 18: Analog video DAC pins

Pin	Location	I/O	Function
ROUT	AF11	O	Red output
GOUT	AE11	O	Green output
BOUT	AD12	O	Blue output
COUT	AF9	O	Chroma output
CVOUT	AD10	O	Composite video output
YOUT	AE10	O	Luma output

Table 19: Digital video pins

Pin	Location	I/O	Function	Pad type
NOT_HSYNC[A]	AE20	I/O	Horizontal sync	C4
EVENNOTODD[a]	AF20	I/O	Vertical sync	C4

a. 5 V tolerant

2.6.3. Pin Description (Continued)

Table 20: Port 0 PIO signal assignments

Port 0 bit	Input	Output
Bit 0		SC0_DATAOUT or ASC0_TXD[a]
Bit 1	SC0_DATAIN or ASC0_RXD[a]	
Bit 2	SC0_CG_EXTCLK	
Bit 3		SC0CG_CLK or SMCDSS_CLK[b]
Bit 4		(SCO_RESET)
Bit 5		(SC0_NOT_SETVCC)
Bit 6		SC0_DIR or ASC0_NOTOE[c], (SC0_NOT_SETVPP)
Bit 7	(SC0_DETECT)	

a. ASC0 TX/RX data becomes smartcard TX/RX data when the ASC module is used in smartcard mode.

b. Output function between PIO or smartcard module clock generator alternate function and clock generator module frequency synthesizer clock is selected by bit 28 in the interconnect register CONFIG_CONTROL_A (SMCARDA_DSSSMCLK_NOT_PIOBIT3). If the DSS smartcard mode is selected (bit 28 = 1), this overrides the normal PIO or PIO alternate function output.

c. When ASC0 is used in nonsmartcard mode, the smartcard direction signal becomes an active low ASC TX output enable signal. The signals are in fact the same, that is, SC0_DIR = 0 means smartcard TX is active.

Table 21: Port 1 PIO signal assignments

Port 1 bit	Input	Output
Bit 0		SC1_DATAOUT or ASC1_TXD[a]
Bit 1	SC1_DATAIN or ASC1_RXD[a]	
Bit 2	SC1_CG_EXTCLK	
Bit 3		SC1CG_CLK or SMCDSS_CLK[b]
Bit 4		(SC1_RESET)
Bit 5	YC[1]	YC[1], (SC1_NOT_SETVCC)
Bit 6		SC1_DIR or ASC1_NOTOE[c], (SC1_NOT_SETVPP)
Bit 7	YC[0] (SC1_DETECT)	YC[0]

a. ASC1 TX/RX data becomes smartcard TX/RX data when the ASC module is used in smartcard mode.

b. Output function between PIO or smartcard module clock generator alternate function and clock generator module frequency synthesizer clock is selected by bit 29 in the interconnect register CONFIG_CONTROL_A (SMCARDB_DSSSMCLK_NOT_PIOBIT3). If the DSS smartcard mode is selected (bit 29 = 1) this overrides the normal PIO or PIO alternate function output.

c. When ASC1 is used in nonsmartcard mode the smartcard direction signal becomes an active low ASC TX output enable signal. The signals are in fact the same, that is, SC1 DIR = 0

2.6.3. Pin Description (Continued)

Table 22: Port 2 PIO signal assignments

Port 2 bit	Input	Output
Bit 0		MAFE_HC1 or NOT_ASC4_RTS[a]
Bit 1		MAFE_DOUT or ASC4_TXD[a]
Bit 2	MAFE_DIN or ASC4_RXD[a]	
Bit 3	MAFE_FS or NOT_ASC4_CTS[a]	
Bit 4	MAFE_SCLK	
Bit 5	PWM_CAPTURE0	
Bit 6		PWM_COMPARE0
Bit 7		PWM_OUT0

a. Controlled by bit MAFE_OR_UART4_SEL in interconnect register CONFIG_CONTROL_D (bit 20).

Table 23: Port 3 PIO signal assignments

Port 3 bit	Input	Output
Bit 0	SSC0_MTSR_DIN or SSC0_MRST_DIN	SSC0_MTSR_DOUT or SSC0_MRST_DOUT[a]
Bit 1	SSC0_SCLKIN	SSC0_SCLKOUT
Bit 2	SSC1_MTSR_DIN or SSC1_MRST_DIN	SSC1_MTSR_DOUT or SSC1_MRST_DOUT[b]
Bit 3	SSC1_SCLK	SSC1_SCLK
Bit 4	NOT_CD_REQ[0] or PCMI_LRCLK	I1284PERILOGICHIGH
Bit 5	Slave mode I1284HOSTLOGICHIGH or PCMI_DATA	Master mode I1284HOSTLOGICHIGH
Bit 6	NOT_CD_REQ[1] or PCMI_SCLK	I1284INNOTOUT
Bit 7		PWM_OUT1

a. Output function selected by bit 24 in interconnect configuration register CONFIG_CONTROL_B (COMMS_SSC0_DOUT_MRST_NOTMTSR_MUXSEL)

b. Output function selected by bit 25 in interconnect configuration register CONFIG_CONTROL_B (COMMS_SSC1_DOUT_MRST_NOTMTSR_MUXSEL)

2.6.3. Pin Description (Continued)

Table 24: Port 4 PIO signal assignments

Port 4 bit	Input	Output
Bit 0	TTXTREQUEST or OSDENABLE	OSDENABLE[a]
Bit 1	CFC	TXTDATAOUT[b]
Bit 2	YC[7]	YC[7]
Bit 3	ASC2_RXD	
Bit 4		ASC2_TXD [c]
Bit 5	PWM_CAPTURE2 or YC[6]	YC[6]
Bit 6	SCCG_EXTCLK	PWM_COMPARE2
Bit 7		PWM_OUT2

a. OSDENABLE output function is selected rather than PIO by interconnect configuration register CONFIG_CONTROL_C, bit 2 (CONFIG_OTHER_ALT_PIOPORT4[0]). The output can then be turned off by the MPEG video decoder to use OSDENABLE as an input.

b. TXTDATAOUT function selected by interconnect configuration register CONFIG_CONTROL_C, bit 3 (CONFIG_OTHER_ALT_PIOPORT4[1])

c. After reset, register CONFIG_CONTROL_C bit 4 must be set to 1 to pass PIO data or to use ASC2_TXD in alternate output PIO mode.

Table 25: Port 5 PIO signal assignments

Port 5 bit	Input	Output
Bit 0	IRB_IR_IN[a]	
Bit 1	IRB_UHF_IN[b]	
Bit 2		Infrared transmitter/receiver drive PPM
Bit 3		Infrared transmitter/receiver drive jack (0 or z) open drain jack output [c, d]
Bit 4	YC[5]	ASC3_TXD or YC[5][e]
Bit 5	ASC3_RXD or YC[4]	YC[4]
Bit 6	NOT_ASC3_CTS or YC[3]	YC[3]
Bit 7	YC[2]	NOT_ASC3RTS or YC[2][e]

a. The wake-up from low power mode function is enabled by interconnect configuration register CONFIG_CONTROL_D, bit 21 (RC_IRDA_DATA_IN_EN).

b. The wake-up from low power mode function is enabled by interconnect configuration register CONFIG_CONTROL_D, bit 22 (UHF_IN_EN).

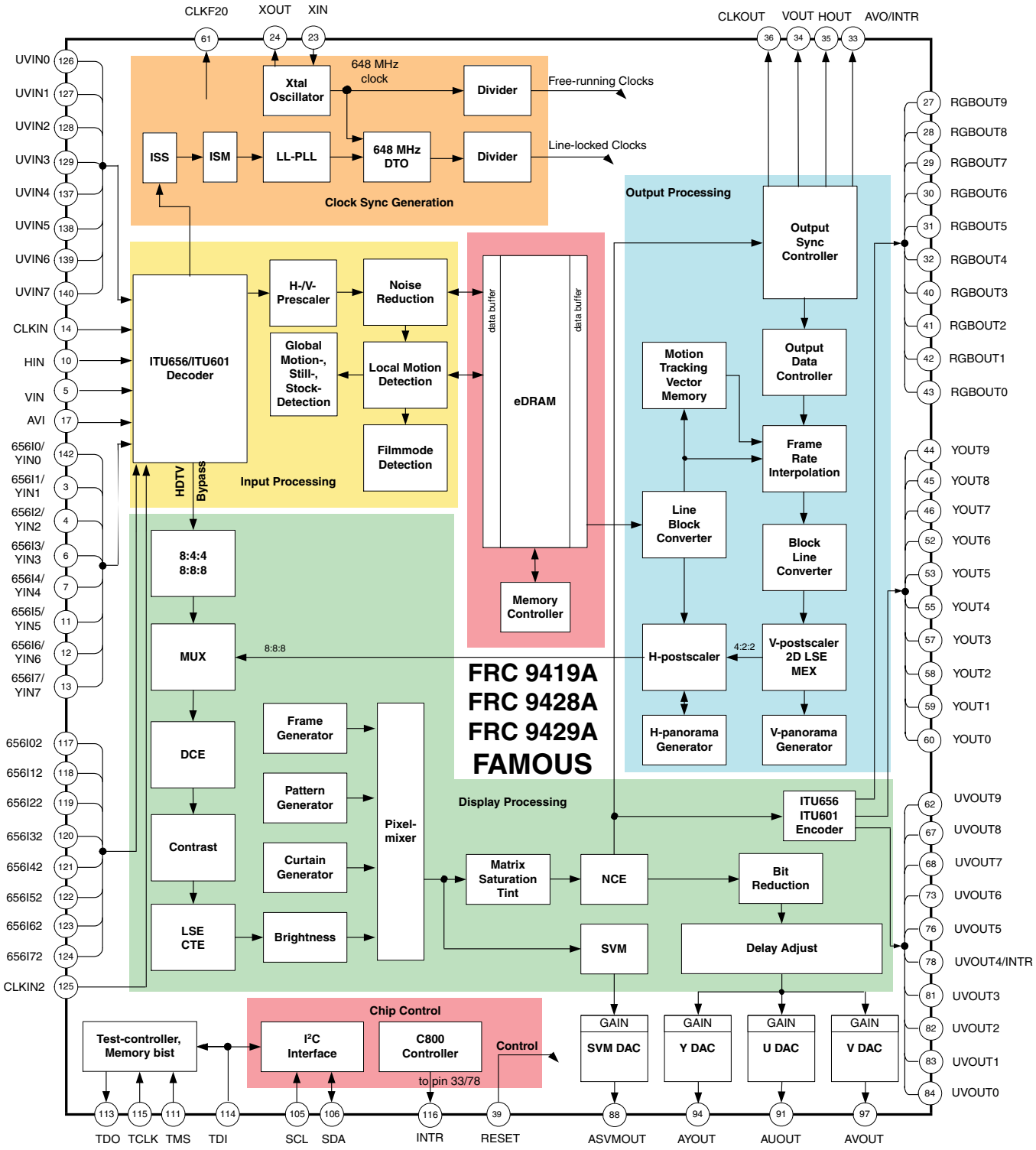
c. PIO needs to be configured as open drain in alternate output mode to use infrared transmitter/receiver drive jack.

d. After reset, bit 5 in CONFIG_CONTROL_C must be set to 1 to pass PIO data or use infrared transmitter/receiver drive jack in alternate function mode.

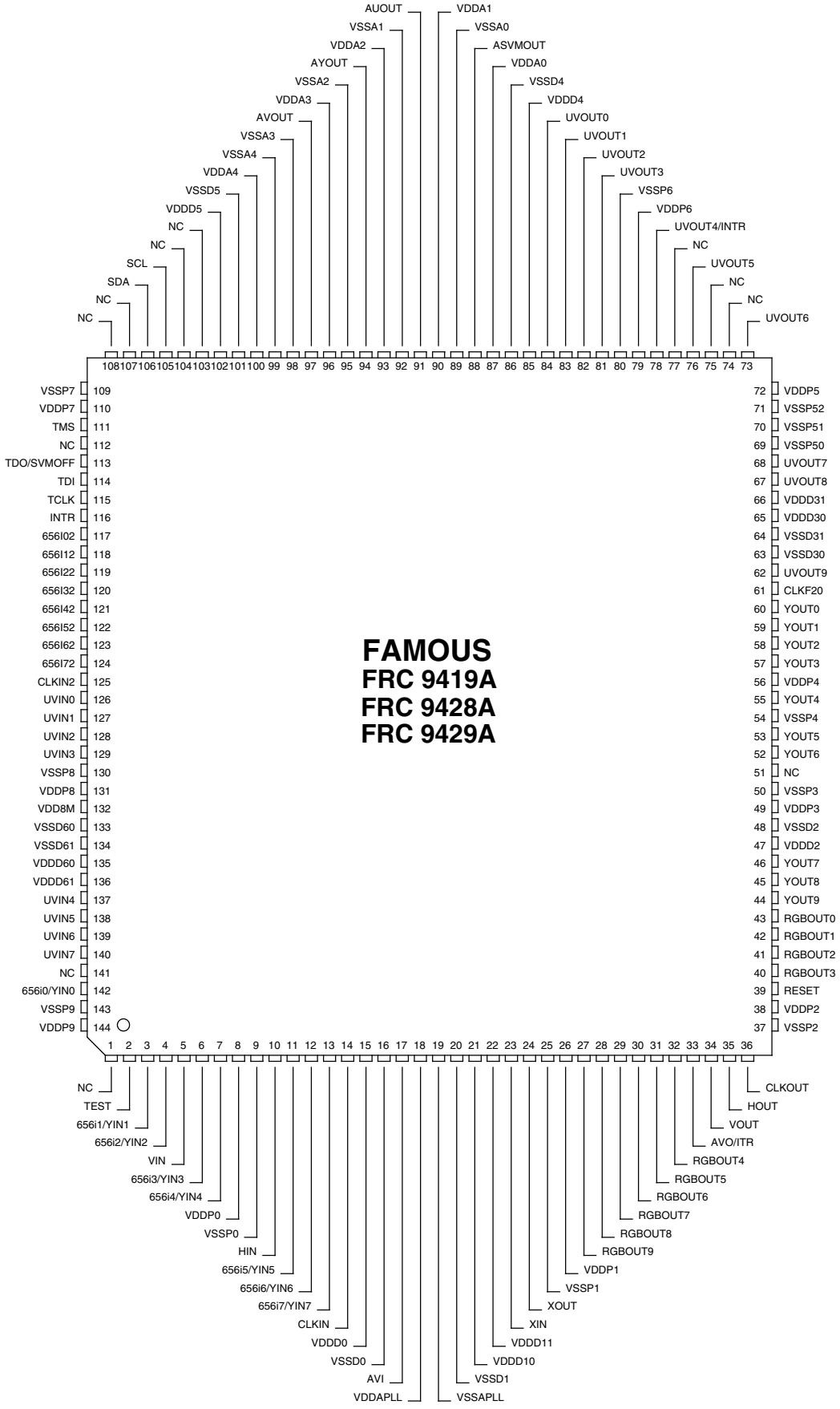
e. Output function selected by bit 11 in CONFIG_CONTROL_E (CONFIG_OTHER_ALT_PIO_YC)

2.7. IC3301 (RH-IXB064WJN1Q)

2.7.1. FRC Block Diagram

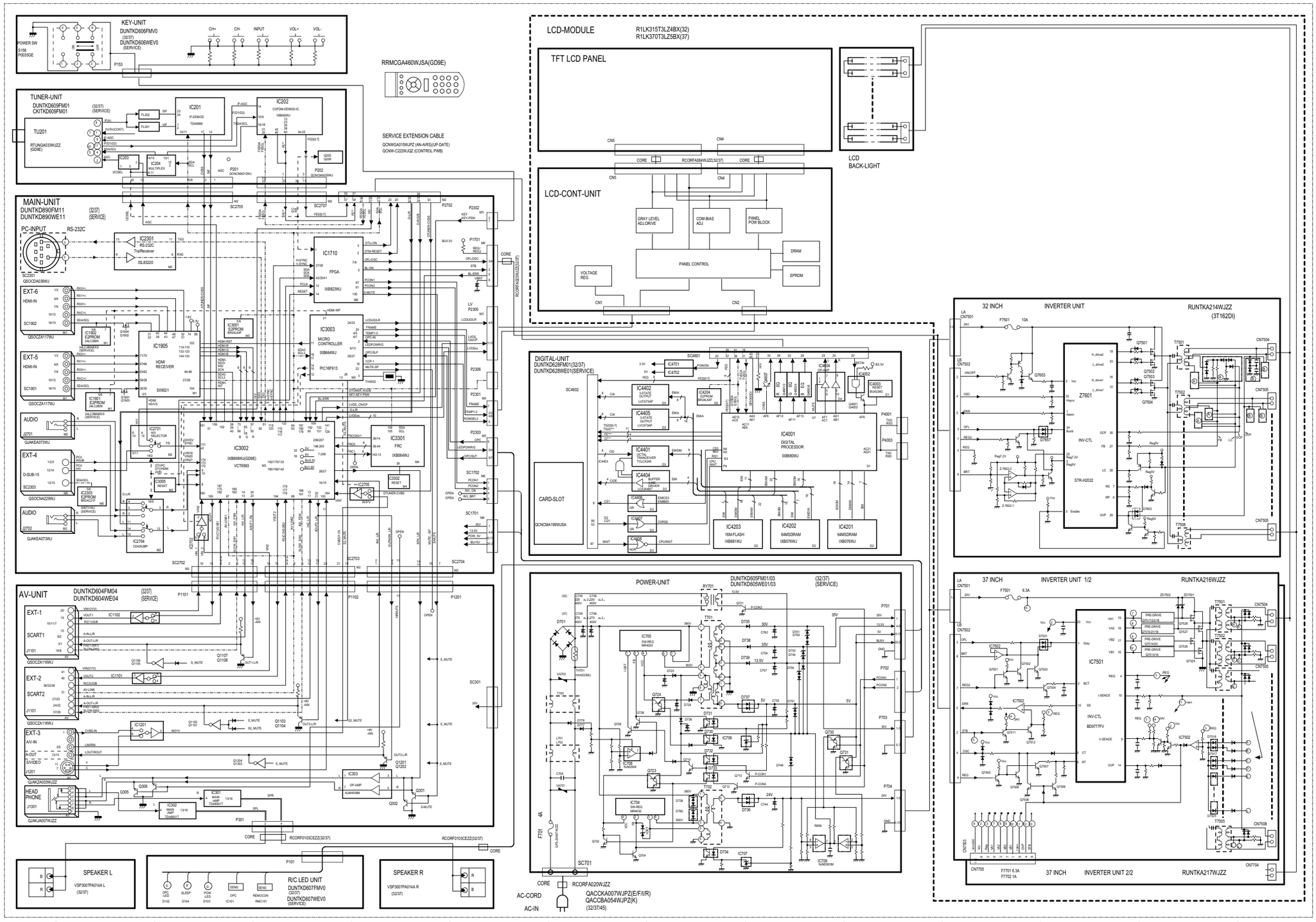


2.7.2. FRC Pinning

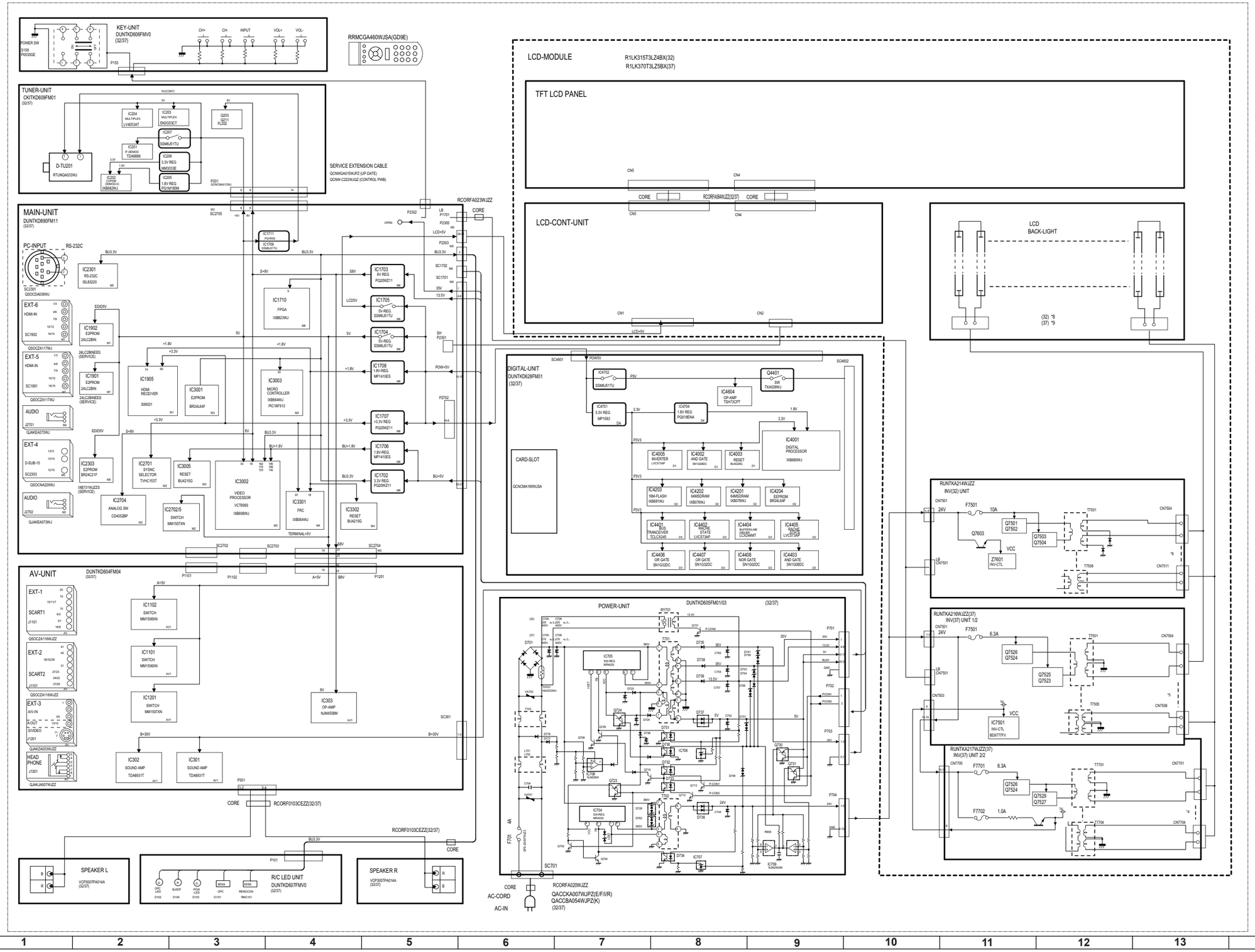


BLOCK DIAGRAM

System Block Diagram



Power-Source Block Diagram



SCHEMATIC DIAGRAMS

Description:

VOLTAGE MEASUREMENT CONDITION:

1. The voltages at test points are measured on exclusive AC adaptor and the stable supply voltage of AC 230V. Signals are fed by a color bar signal generator for servicing purpose and the above voltages are measured with a 20k ohm/V tester.

INDICATION OF RESISTOR & CAPACITOR:

RESISTOR

1. The unit of resistance "Ω" is omitted. (K=kΩ=1000 Ω, M=MΩ).
2. All resistors are ± 5%, unless otherwise noted. (J= ± 5%, F= ± 1%, D= ± 0.5%)
3. All resistors are 1/16W, unless otherwise noted.
4. All resistors are Carbon type, unless otherwise noted.

Ⓒ: Solid Ⓦ: Cement
Ⓢ: Oxide Film Ⓣ: Special
Ⓝ: Metal Coating

CAPACITOR

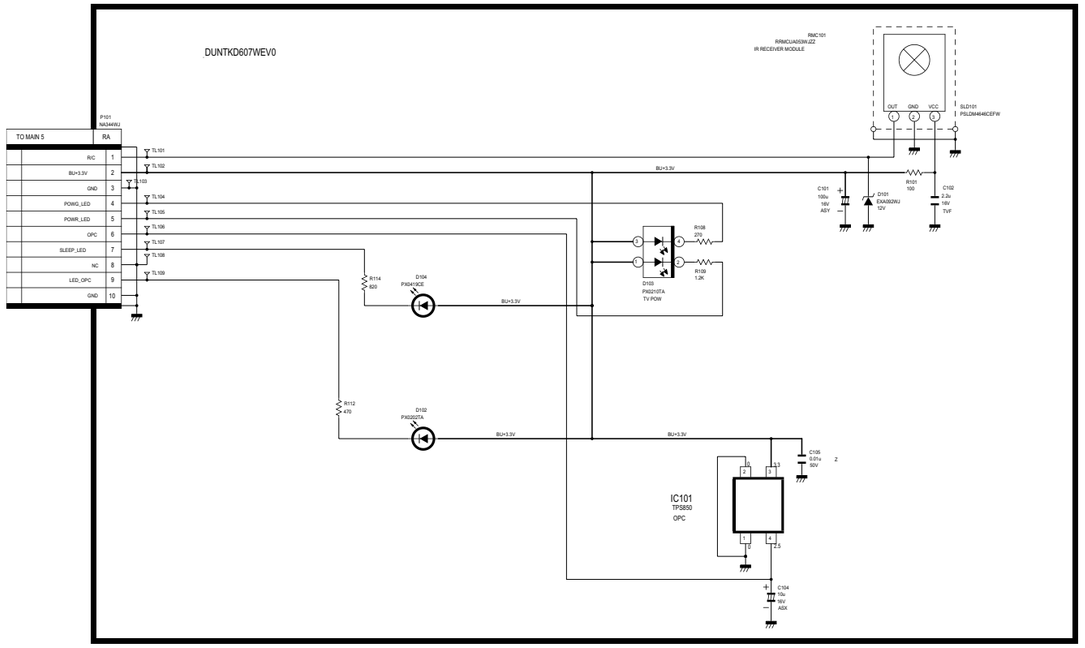
1. All capacitors are μF, unless otherwise noted. (P=pF=μμ F).
2. All capacitors are 50V, unless otherwise noted.
3. All capacitors are Ceramic type, unless otherwise noted.

(ML): Mylar (TA): Tantalum
(PF): Polypro Film (ST): Styrol

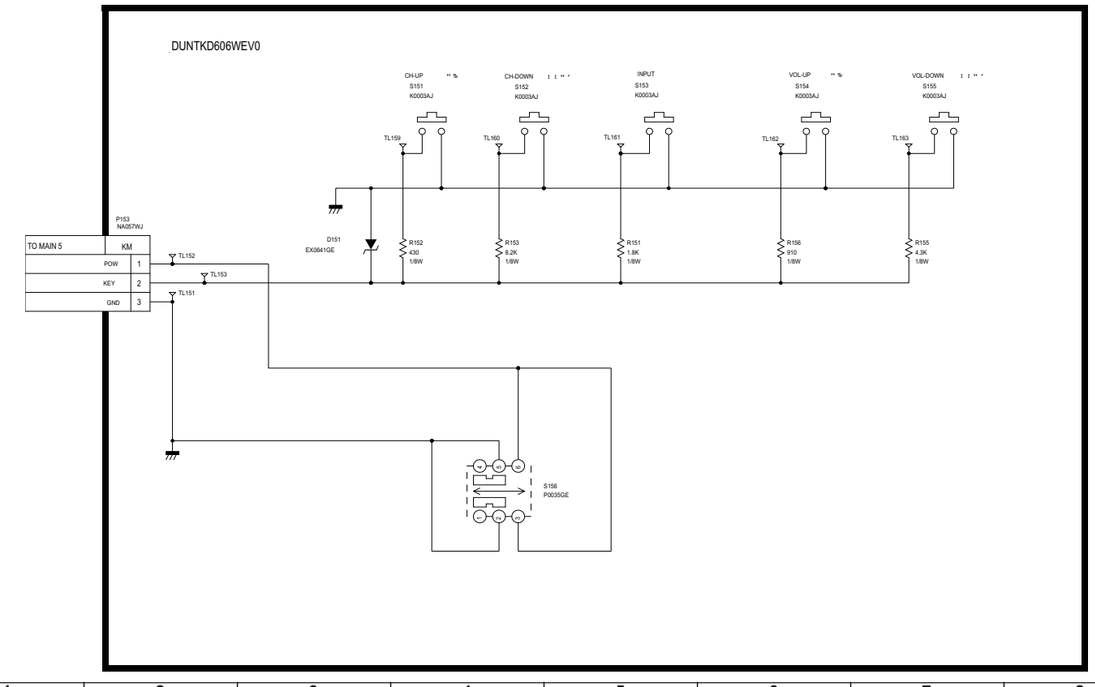
CAUTION:
This circuit diagram is original one, therefore there may be a slight difference from yours.

IMPORTANT SAFETY NOTICE:
PARTS MARKED WITH "⚠" ( ) ARE IMPORTANT FOR MAINTAINING THE SAFETY OF THE SET. BE SURE TO REPLACE THESE PARTS WITH SPECIFIED ONES FOR MAINTAINING THE SAFETY AND PERFORMANCE OF THE SET.

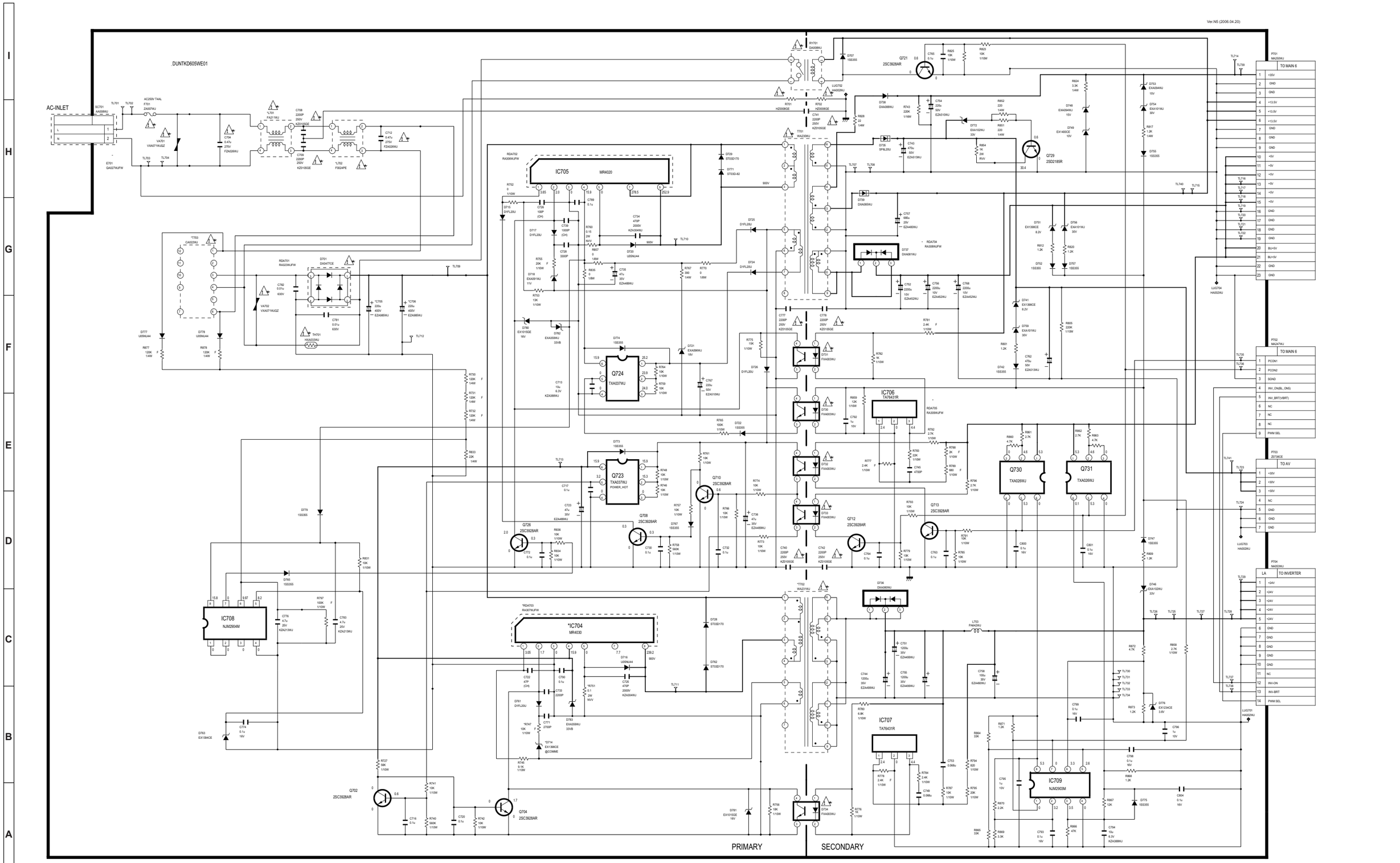
LC-32/37GD9E RC/LED Unit Diagram



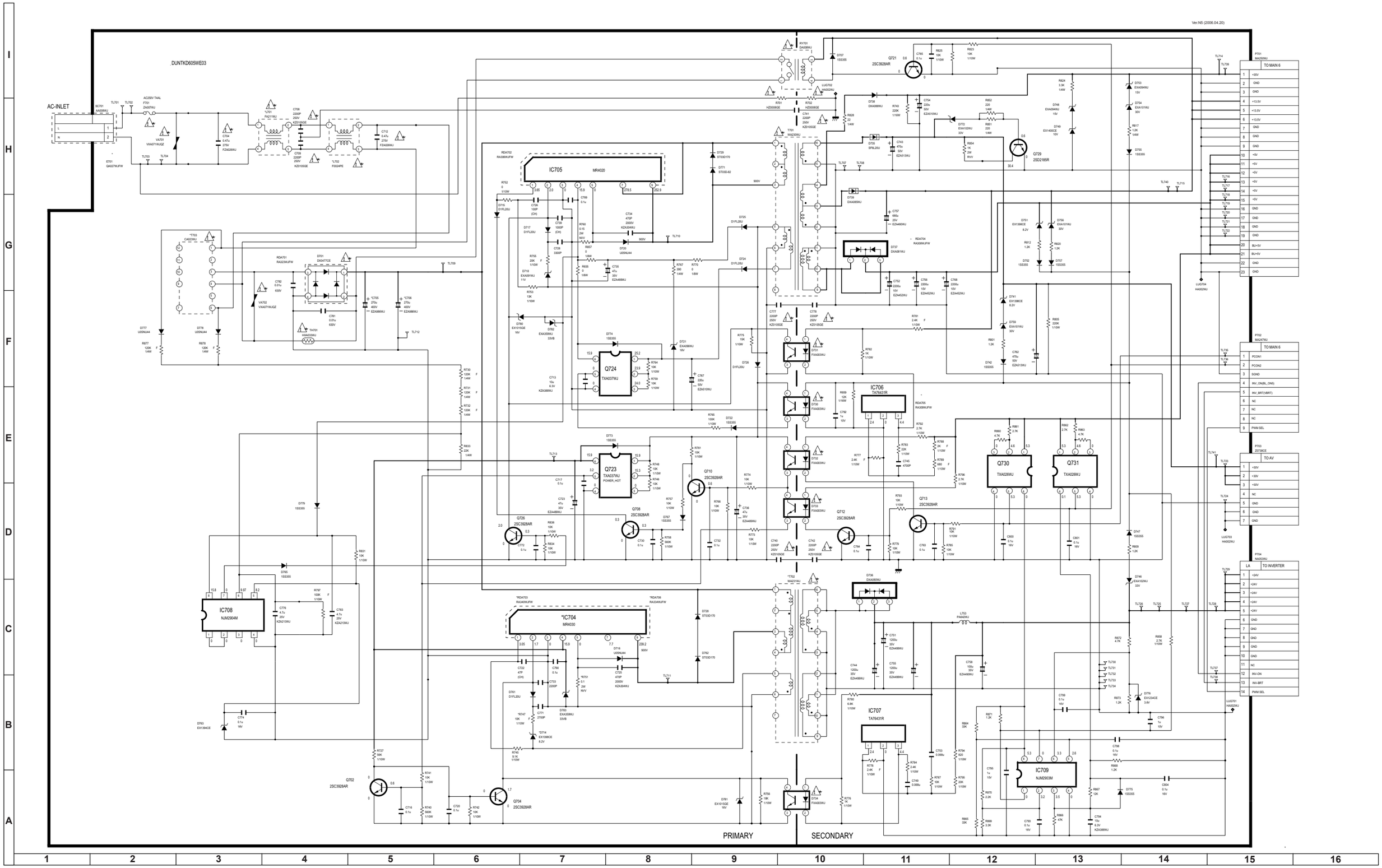
LC-32/37GD9E KEY Unit Diagram



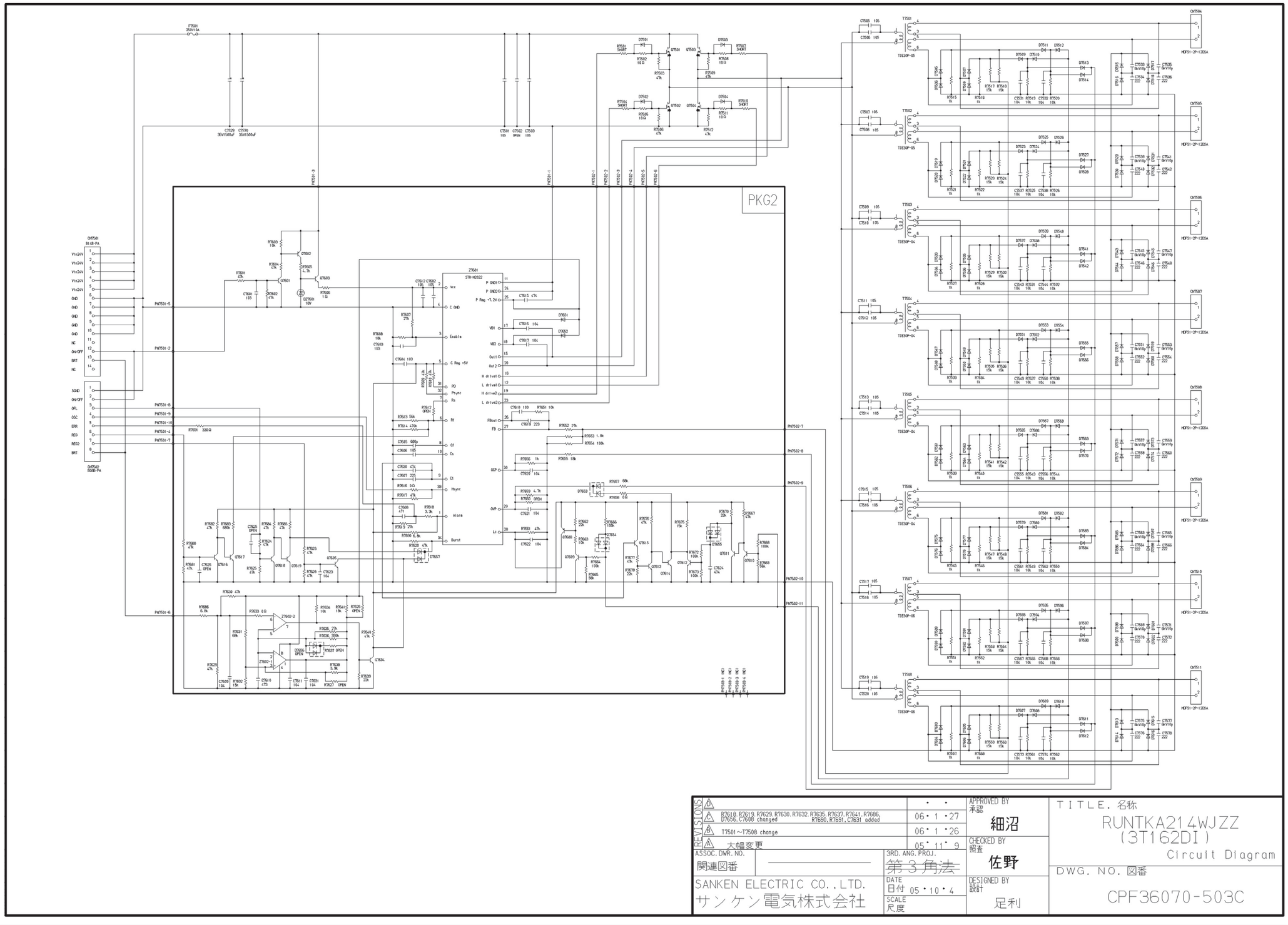
LC-32GD9E POWER SUPPLY Unit Diagram



LC-37GD9E POWER SUPPLY Unit Diagram



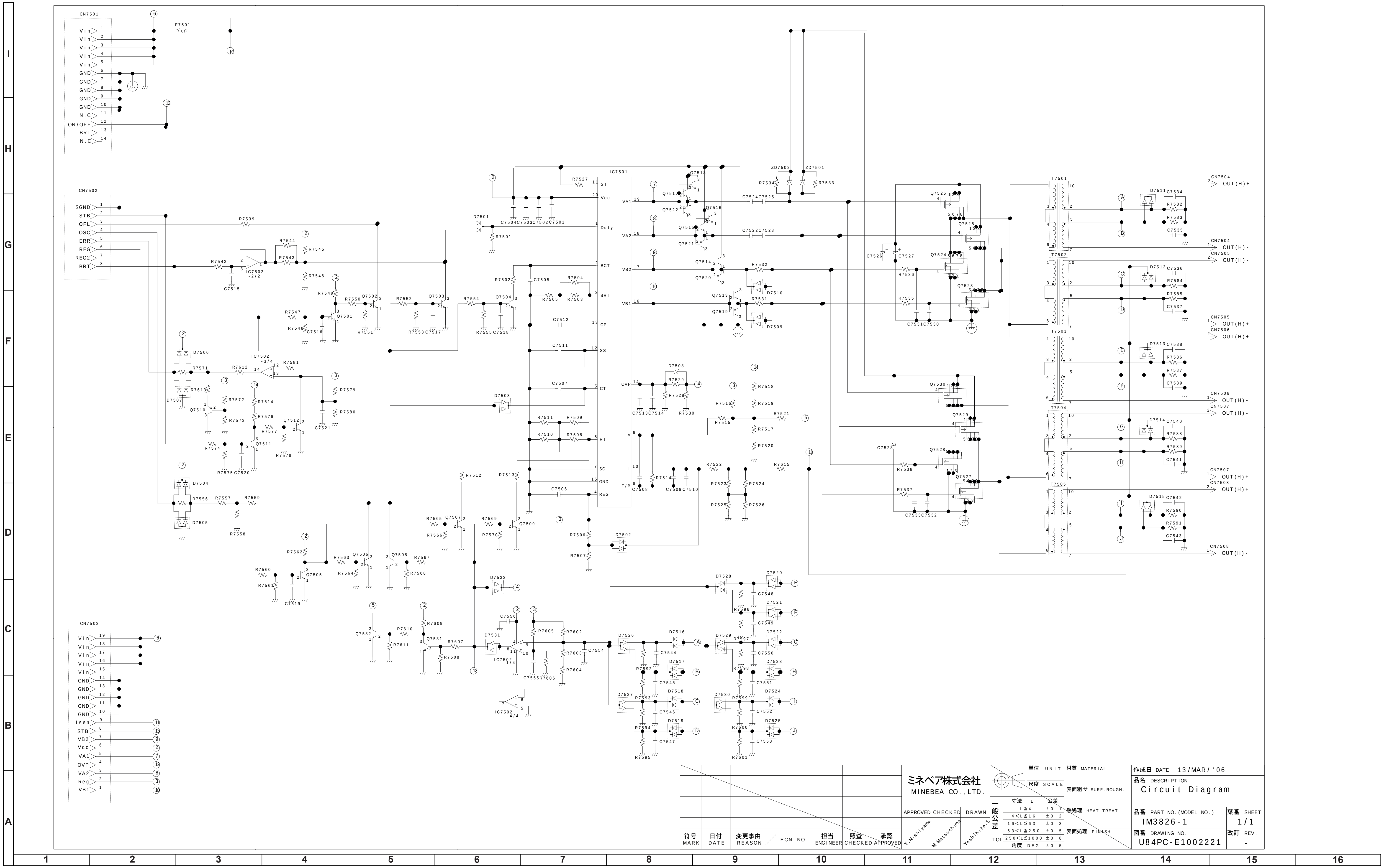
LC-32GD9E INVERTER Unit Diagram (RUNTKA214WJZZ)



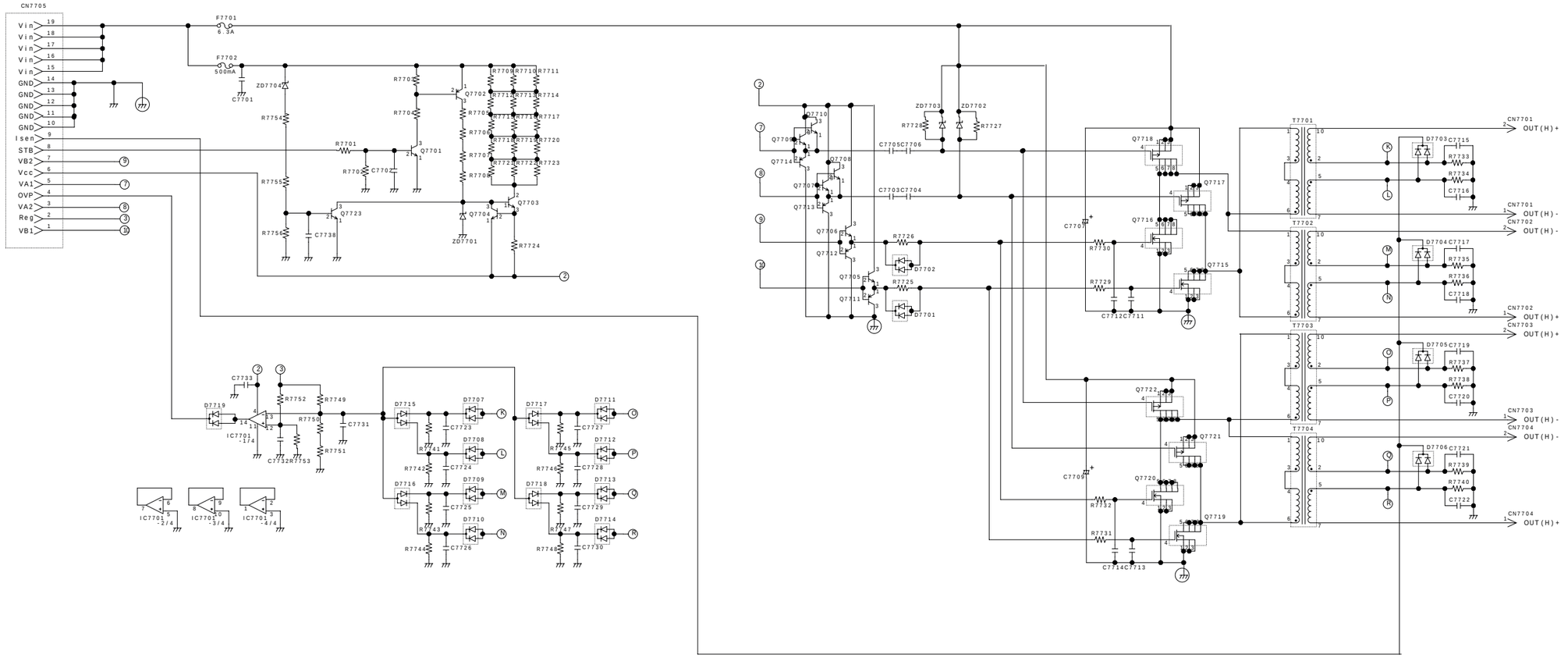
REVISIONS			
A	R7618 R7619 R7629 R7630 R7632 R7635 R7637 R7641 R7686, D7656, C7608 changed	06・1・27	APPROVED BY 承認 細沼
B	T7501～T7508 change	06・1・26	CHECKED BY 照査 佐野
A	大幅変更	05・11・9	DESIGNED BY 設計 足利

ASSOC. DWR. NO. 関連図番		3RD. ANG. PROJ. 第3角法	TITLE. 名称 RUNTKA214WJZZ (3T162DI) Circuit Diagram
SANKEN ELECTRIC CO.,LTD. サンケン電気株式会社		DATE 日付 05・10・4	DWG. NO. 図番 CPF36070-503C
		SCALE 尺度	

LC-37GD9E INVERTER Unit Diagram (RUNTKA216WJZZ)



LC-37GD9E INVERTER Unit Diagram (RUNTKA217WJZZ)



符号 MARK	日付 DATE	変更事由 REASON / ECN NO.	担当 ENGINEER	照査 CHECKED	承認 APPROVED

ミネベア株式会社
MINEBEA CO.,LTD.

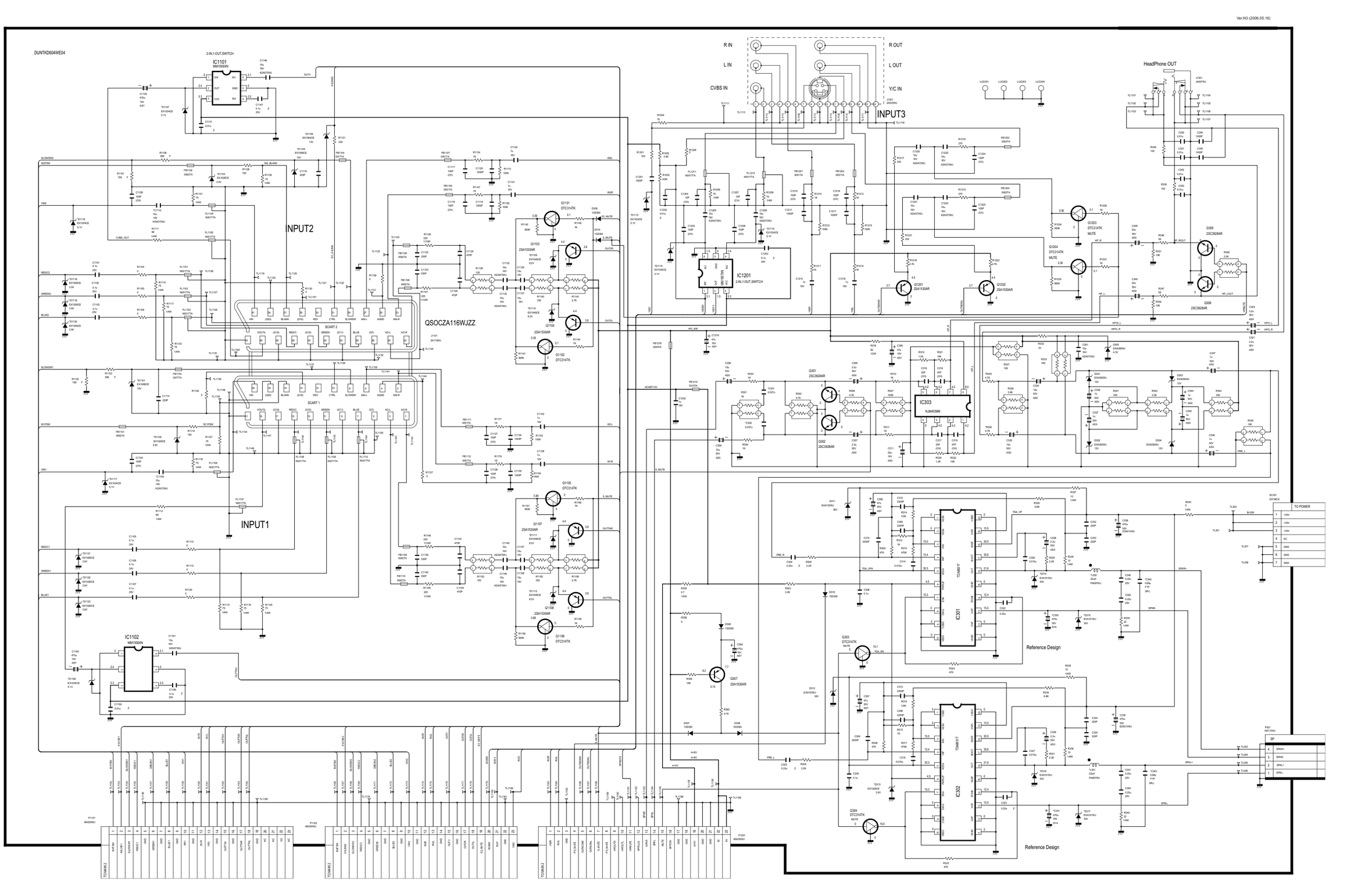
	APPROVED	CHECKED	DRAWN
	T.Nishiyama	M.Matsushima	Yoshihiro.S

一般公差 TOL	寸法 L	公差
	L≦4	±0.1
	4<L≦16	±0.2
	16<L≦63	±0.3
	63<L≦250	±0.5
	250<L≦1000	±0.8
	角度 DEG	±0.5

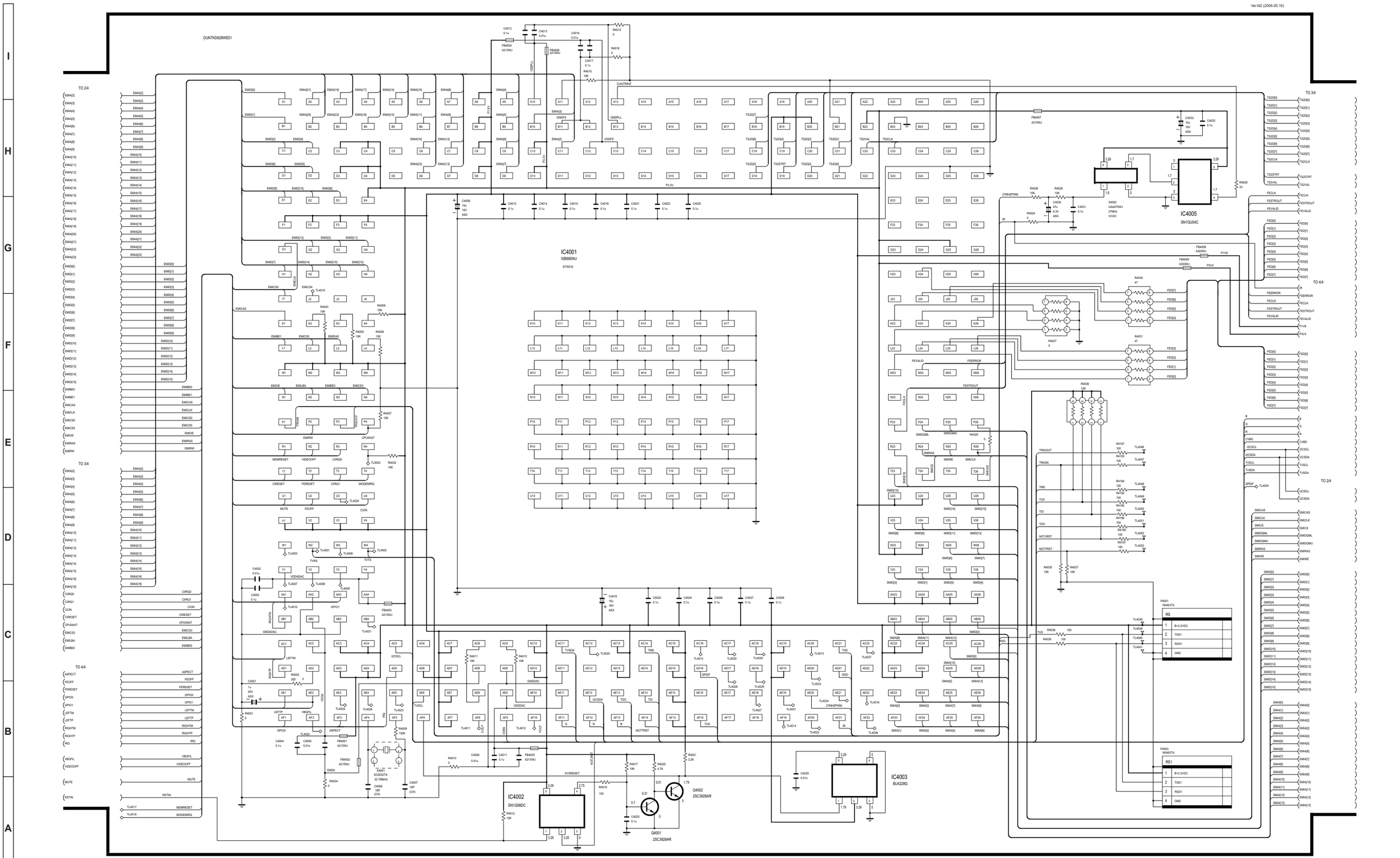
単位 UNIT	
尺度 SCALE	
材質 MATERIAL	
表面粗サ SURF.ROUGH.	
熱処理 HEAT TREAT	
表面処理 FINISH	
作成日 DATE	13/MAR/'06
品名 DESCRIPTION	Circuit Diagram
品番 PART NO.(MODEL NO.)	IM3826-2
葉番 SHEET	1/1
図番 DRAWING NO.	U84PC-E1003119
改訂 REV.	-

LC-32/37GD9E AV Unit Diagram

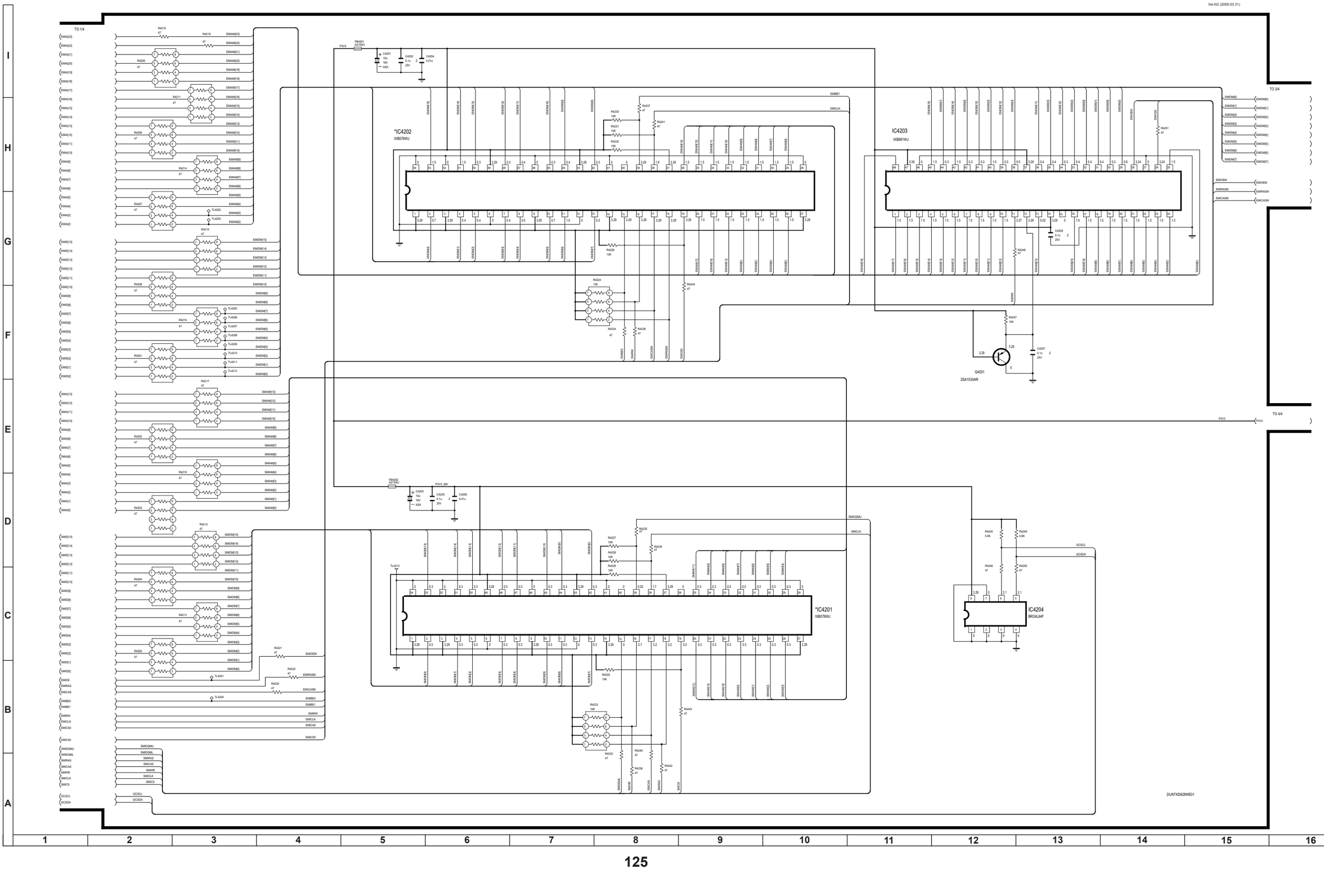
Ver.N3 (2006.05.16)



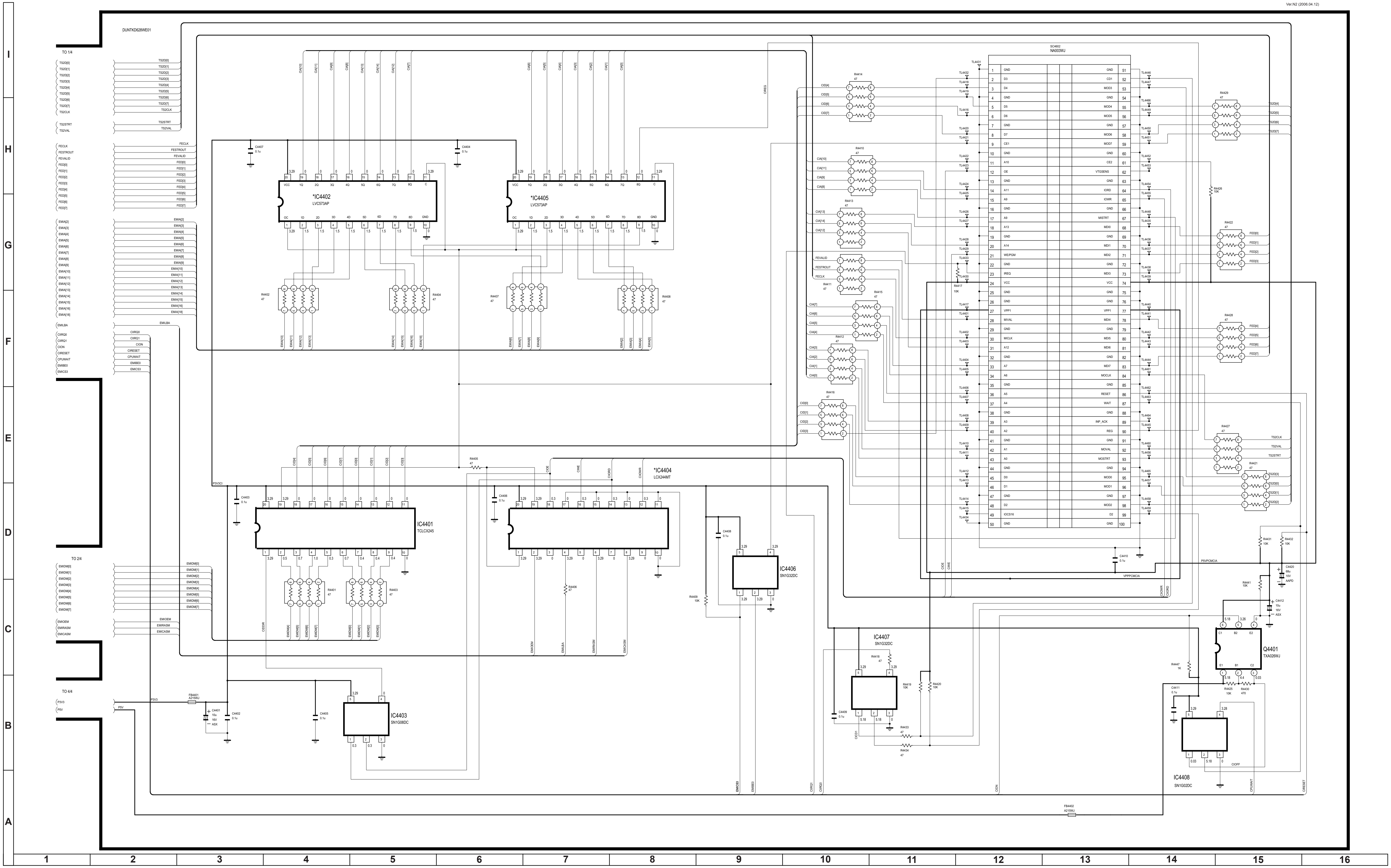
LC-32/37GD9E Digital Unit Diagram 1/4 (STI5516)



LC-32/37GD9E Digital Unit Diagram 2/4 (MEMORIES)



LC-32/37GD9E Digital Unit Diagram 3/4 (CI)



LC-32/37GD9E Digital Unit Diagram 4/4 (AUDIO / VIDEO OUT / REG)

Ver.N2 (2006.04.12)

DUNTKD628WE01

IC4704
PQ018ENA

IC4701
MP1583
DC-DC 3.3V

IC4702
SSM6J51TU

IC4604
TSH73CPT

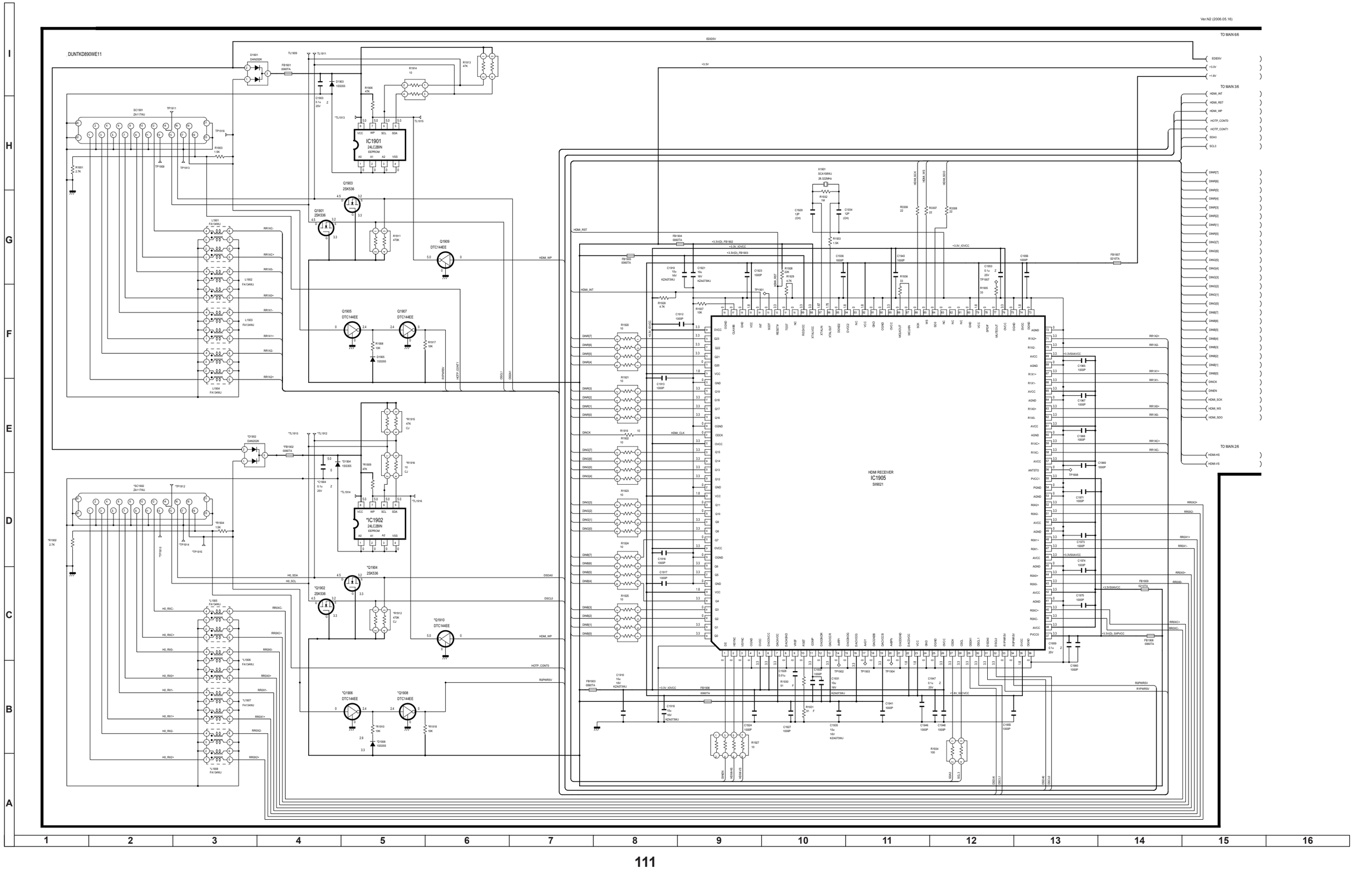
SC4601
WA2022WJ
TO MAIN

2	GND			+12V	1
4	GND			+12V	3
6	+5V			GND	5
8	+5V			GND	7
10	+5V			GND	9
12	+5V			GND	11
14	+5V			GND	13
16	+5V			GND	15
18	GND			ASPECT	17
20	RESETn			SCL	19
22	IRQ			SDA	21
24	R			POWON	23
26	GND			L	25
28	BLUE			V	27
30	GND			H	29
32	GREEN			GND	31
34	GND			CVBS	33
36	RED			GND	35
38	GND			FERESETn	37
40	FEOFF_X4M			FESCL	39
42	GND			FESDA	41
44	FESTR_PSYNC			FEGPO_COMP	43
46	FEVAL_DEN			FEGP1_LOCK	45
48	GND			FEERR_UNCOR	47
50	FED0			GND	49
52	FED2			FED1	51
54	FED4			FED3	53
56	FED6			FED5	55
58	FECLK			FED7	57
60	GND			GND	59

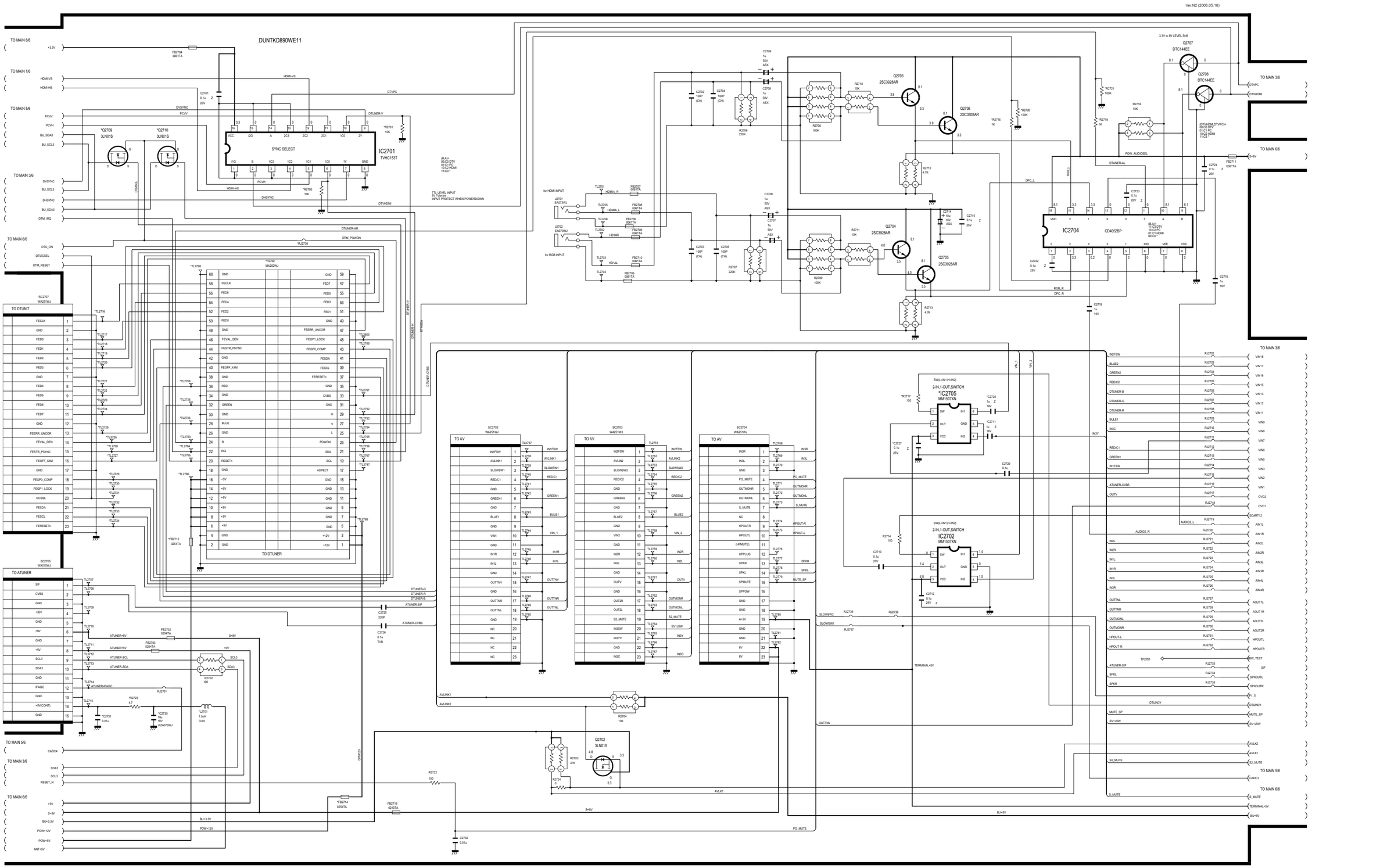
TO 3/4 (5V)
TO 1/4
TO 2/4
TO 3/4
TO 1/4
TO 1/4

I																
H																
G																
F																
E																
D																
C																
B																
A																
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

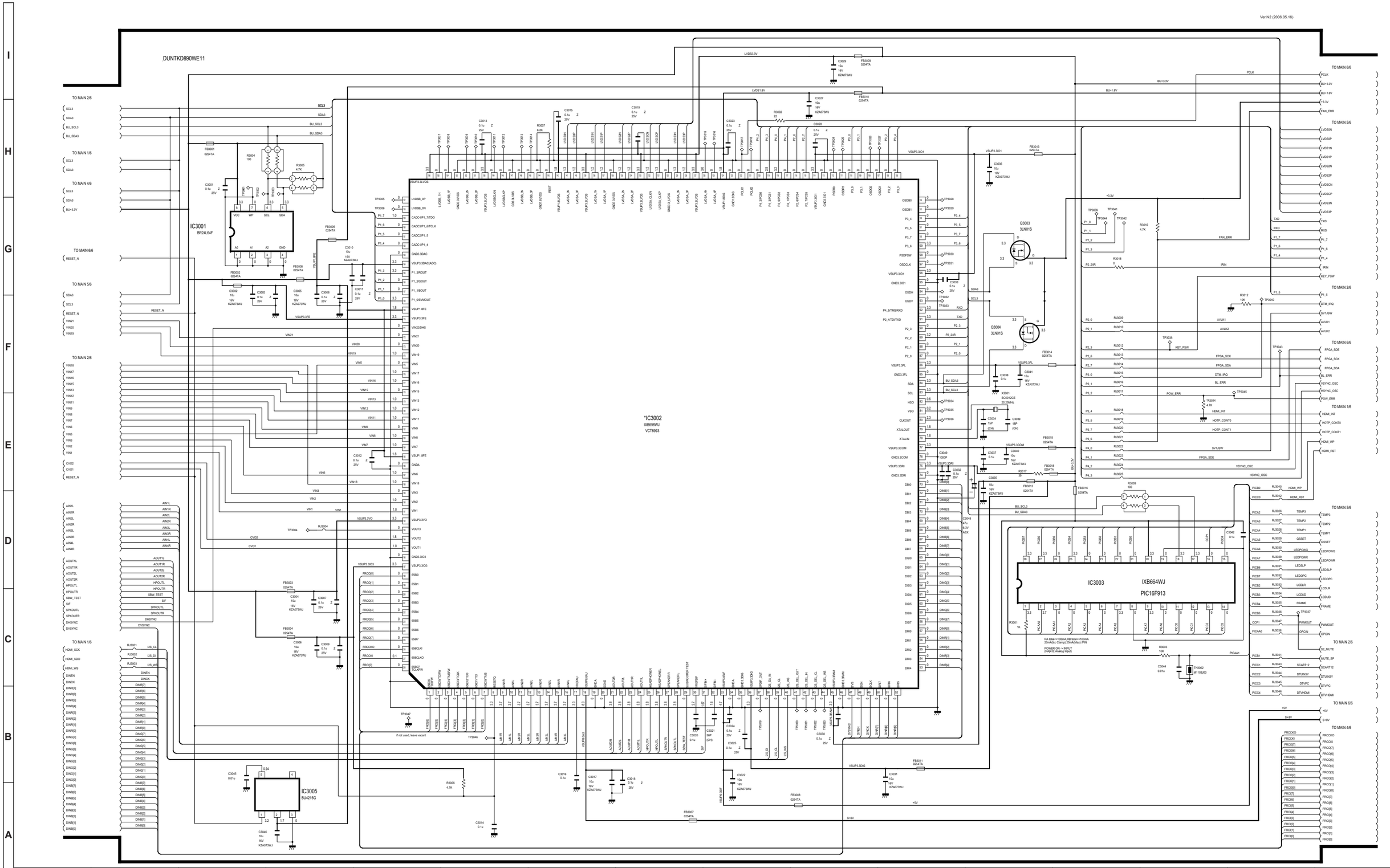
LC-32/37GD9E Main Unit Diagram 1/6 (HDMI)



LC-32/37GD9E Main Unit Diagram 2/6 (Signal IN OUT)



LC-32/37GD9E Main Unit Diagram 3/6 (VCTP)



LC-32/37GD9E Main Unit Diagram 4/6 (FRC)

Ver.N2 (2006.05.16)

DUNTKD890WE11

*IC3301
IXB064WJN1

*IC3303
TC7SA08U

*IC3304
TC7SA08U

*IC3302
BU4215G

TO MAIN 3/6

TO MAIN 6/6

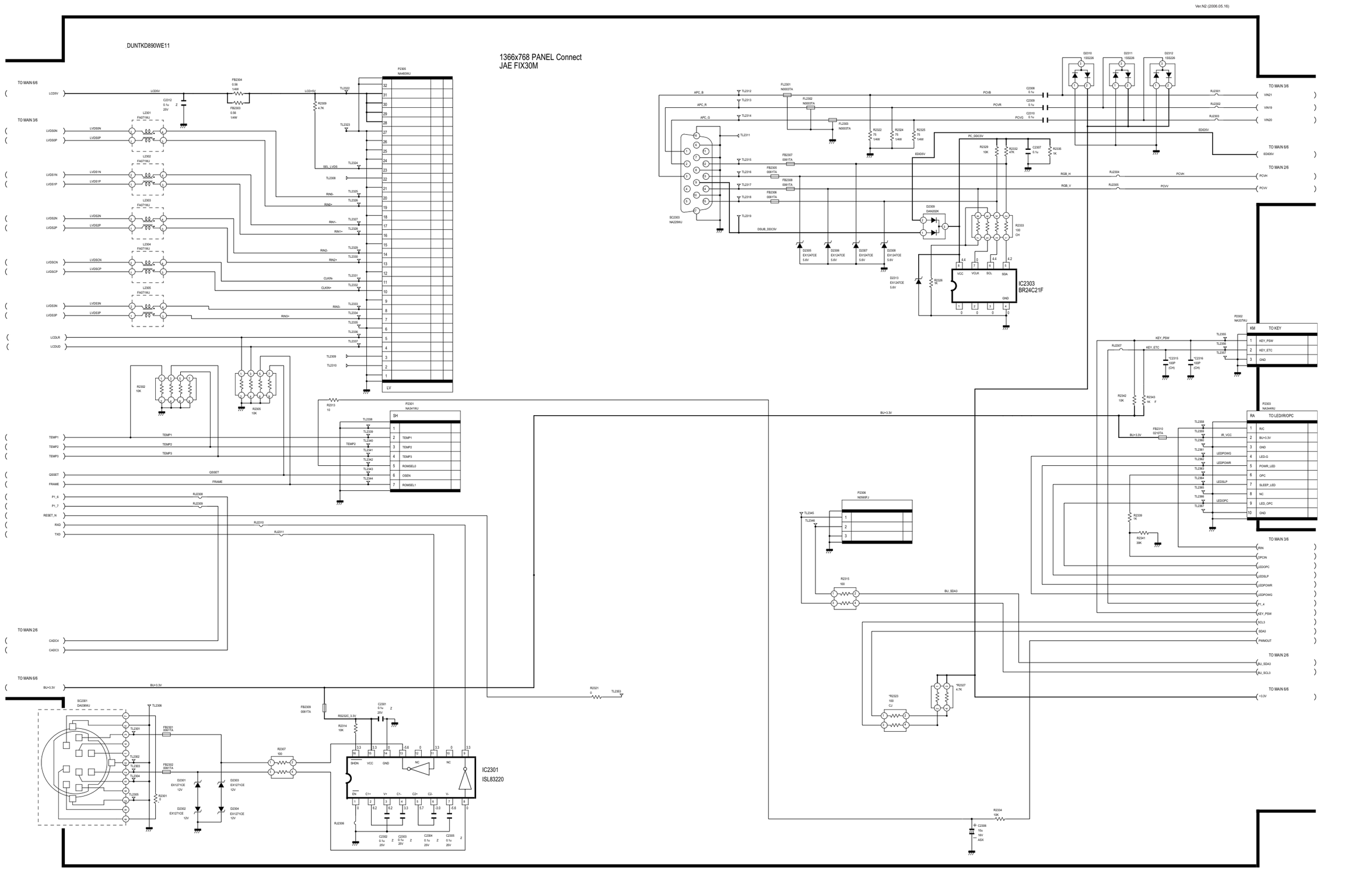
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

LC-32/37GD9E Main Unit Diagram 5/6 (MISC)

Ver.N2 (2006.05.16)

DUNTKD890WE11

1366x768 PANEL Connect
JAE FIX30M



LC-32/37GD9E Main Unit Diagram 6/6 (POWER DC-DC)